

## A 7-level inverter with less number of switches for grid-tied PV applications

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### Abstract

*In the current context, Medium Voltage High Power (MVHP) applications are developing industrial technologies. The direct connection of a Photovoltaic (PV) system to an MVHP system may cause various connectivity challenges. To address the interconnection difficulties, this paper describes a 7-Level Cascaded H-Bridge Multilevel Inverter (CHB-MLI) architecture with fewer switches and lower harmonics. This article proposes the Reduced Switch Multilevel Inverter (RSMLI). This design is less expensive than traditional Multilevel Inverter (MLI) topologies, and it is ideally suited for medium voltage and high-power applications since it synthesizes numerous Direct Current (DC) sources. The innovative 7-Level inverter is represented with a decreased number of switches using the Phase Opposition Disposition (POD) methodology. The lower switch count helps the construction of simple converter structures. To boost performance, the MATLAB/Simulink results are evaluated.*

### Keywords

*Multilevel inverter (MLI), Pulse width modulation (PWM), Phase opposition disposition (POD), Photovoltaic (PV) systems, Reduced switch components (RSC), Total harmonic distortion (THD).*

### 1. Introduction

Because of the massive power demand and fast increase of industrial needs, traditional power production is falling behind. The negative impacts of conventional power production have pushed technology toward renewable energy sources, with solar power being an ample supply for current and future demands [1]. Medium voltage grid utility applications need the use of medium voltage and megawatt power levels. Stand-alone renewable energy systems, particularly Photovoltaic (PV) systems with micro grid and uninterruptible power supply systems, need output voltages with excellent power quality characteristics, such as low total harmonic distortion and quick dynamic response [2]. The primary issue here is the control approach for the Direct Current (DC) -DC converter and the DC-AC inverter. This issue is solved via Multiple Maximum Power Point Tracking (MPPT) and Cascaded H-bridge (CHB) algorithms and topology. In this context, the Multilevel Inverter (MLI) plays an important role in converting DC to Alternating Current (AC), with the number of levels, determining the realisation of pure sinusoidal voltage output [3–4].

As the level of the inverter grows, the Total Harmonic Distortion (THD) decreases, but the number of switches for the inverter grows by. The increasing switches subsequently enhance the complexity of the inverters, thus the greater the number of levels, the more switches. Reduced switch Multilevel Inverter (RSMLI) [5] will solve the issue of additional switches. In this study, an A7-level inverter with fewer switches is investigated in order to achieve reduced THD and higher levels; it employs less switches than a standard inverter. Although obtaining a clean sinusoidal wave from inverters is nearly impossible owing to a variety of reasons. MLI utilised for DC-AC conversion in high power medium voltage applications is classified as follows [6].

- 1) Neutral-Clamped Inverters
- 2) Capacitor-Clamped Inverters
- 3) Cascaded H-bridge Inverters

Because a solar PV system is made up of numerous PV panels, the output voltage of each panel may not be constant and may fluctuate depending on irradiance and meteorological conditions. So, in addition to the neutral clamped and the capacitor clamped inverters, the cascaded H-bridge inverter was selected for the design of the 7-level inverter. Because the cascaded H-

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bridge inverter may be powered by several alternating current sources.

The work is intended:

- To simulate a 7-level inverter for photovoltaic systems using a RSMLI.
- To compare modulation index values at various levels ( $M_a > 1$ ,  $M_a = 1$ ,  $M_a < 1$ ).
- To determine the benefits and limitations, compare its performance to that of an existing converter with RSMLI architecture.
- To investigate and compare THD with R-Load and RL-Load.

## 2. Literature review

Bana et al. [7] provided an overview of reduced switch multilevel inverters and their potential applications in the industry. It compares several features of the RSMLI system, such as switching methodology, controller type, difficulties, and present situation. According to the report, new reduced switch multilevel inverter topologies provide a variety of benefits such as lower cost, lower losses, and smaller space.

Panda et al. [8] A design of Switched Diode Dual Source Single Switch (SDDS) MLI was suggested. The basic goal is to provide the greatest number of outputs while employing the fewest number of switches. The suggested system was compared to ten different systems, and the suggested system had the lowest power loss in the low power range. Also presented a new modified fish swarm optimization (FSO) algorithm that uses the PSO method to reformulate FSO, resulting in a reduction in step values. It outperforms other methods in terms of fitness function minimization. The SDDS MLI is helpful for producing higher level output voltage with fewer switches.

Siddique et al. [9] developed a unique architecture with the goal of achieving greater output levels with fewer switches and a lower total standing voltage. The system generates 13 levels of output using eight unidirectional switches and three DC sources. For the suggested topology, three alternative sorts of extensions are made accessible. In comparison to previous topologies, the suggested topology needs fewer gate driver circuits. A comparison and power loss study have been performed. As a consequence, the topology has a fundamental unit efficiency of 98.5%.

Omer et al. [10] provide a comprehensive overview of some of the most recently suggested multilevel

inverter topologies in several areas. It includes both traditional and freshly suggested topologies. Topologies are reviewed in terms of many factors such as decreased switch count and number of DC sources. It also includes terminology and evaluation criteria. 16 new suggested topologies are chosen, and their comparison, benefits, and disadvantages are provided.

Hosseinpour et al. [11] developed a unique construction for multilayer inverters based on switching diode source cells. It offers bidirectional feeding, inexpensive switch costs, and a low overall blocking voltage. The benefit of this construction is that it only takes one switch diode source cell to enhance the output by two levels. Different parameters have been compared. It features fewer switching losses, fewer switches, and fewer gate driver circuits, resulting in a lower overall cost and a smaller overall system footprint.

Mondol et al. [12] investigated a concept for a novel three-phase multilevel inverter powered by a single energy storage or battery. The staircase modulation approach is used to create switching signals. This architecture features reduced switching losses, allowing the inverter to run at a low switching frequency while maintaining optimum output current harmonic distortion. Finally, since the Total Standing Voltage (TSV) reduces voltage and current levels, the cost of the components is reduced.

Kakar et al. [13] suggested a single phase MLI architecture to minimize the switch count. This architecture has four DC inputs, one bidirectional power switch, and eight unidirectional power switches. The power switches control the higher voltage applications. In the switching strategy, the nearest level is to be utilized.

Srinivasan et al. [14] conducted a thorough study on the decreased switch count for multilayer inverters. A switched ladder inverter may provide 81 different output voltage levels. By raising the magnitude of the DC sources, the number of output levels may be increased. Observe a single-phase induction motor speed with regard to change in load torque when an 81-level inverter is attached.

Singh et al. [15] of a grid-connected Photovoltaic (PV) system with a multilayer inverter. Under continually charged weather circumstances, the Proportional Integral (PI) current regulated algorithm is utilized to calculate Unity Power Factor (UPF). The generated

grid current is sinusoidal, and the PI controller provides an excellent dynamic response.

Sandhu and Thakur [16] demonstrated a hybrid energy system with a 17-level inverter. They demonstrated a model that generates seventeen levels of output by lowering switch count, resulting in greater efficiency and lower THD compared to 9 and 13 levels. They created the model by employing ten Metal–Oxide–Semiconductor Field-Effect Transistor (MOSFET) switches. This artificial neural network (ANN) has been utilized to produce Pulse Width Modulation (PWM) pulses for the inverter. We can obtain a rapid Maximum Power Point (MPP) by utilizing the Artificial Neural Network -Photovoltaics (ANN-PV) technique.

According to Narasimhulu et al. [17], a shunt active power filter adjusts for load current harmonics by injecting harmonic compensating current. The fuzzy logic control is recommended for controlling Shunt Active Power Filter (SAPF). Since it has more control capability. The suggested PI and Fuzzy Logic Controller (FLC) is using Alternate Phase Opposition Disposition (APOD), Phase Opposition Disposition (POD), and Phase Disposition (PD) triangular carriers results in lower THD and higher power factor. We can perform reactive power adjustment utilising the suggested computational intelligence-based controller.

Rajalakshmi and Rangarajan [18] suggested a modified three-phase nine-level multilevel inverter scheme. The number of switches in the multilayer inverter will be lowered by employing this architecture. For symmetrical and asymmetrical DC sources, the suggested topology outperforms the Alternate Phase Opposition Disposition Pulse Width Modulation (APOD-PWM) approach in terms of THD.

Researchers Rana et al. [19] observed that the flying capacitor type multilevel inverter has little benefits over the Diode Clamped Multilevel Inverter (DCMLI) and Cascaded H-bridge Multilevel Inverter (CHBMLI). Increase in voltage between two neighboring electrical drives in Flying Capacitor Multilevel Inverter (FCMLI). The FCMLI is used to decrease switching losses. For balancing the voltage levels of capacitors, phase redundancies are offered in FCMLI.

The Single-Phase Transformer Less Grid-Connected Photovoltaic (SPTG-CPV) inverters are being

reviewed by Zeb et al. [20] Loss analysis for different grid configurations at 1 kW, connected transformer-less inverter topologies are described. The operational principles of all SPTG-CPV inverters are explained in detail for positive, negative, and zero cycles. AC side decoupled topologies such as Highly Efficiency and Reliable Inverter Concept (HERIC), REFU, and Full Bridge Zero Voltage Rectifier (FBZVR) have more efficiency than DC side decoupled topologies such as H5, Full-Bridge Inverter with DC Bypass (FB-DCBP).

### 3. Materials and methods

#### a) System Description

The parts that follow go through the traditional 7-level inverter, the modified 7-level CHB-MLI with reduced switch operation, and total harmonic distortion for 7-level inverters. Sections 4 and 5 offer the POD methodology and Simulink models, respectively, while section 6 presents the outcomes and section 7 discusses data analysis and comments.

#### b) Conventional seven level multilevel inverter topology

The objective of traditional Cascade Multilevel Inverters is to link H-bridges in series with separate DC voltage sources. In MLI, a staircase output voltage (or) current waveform is created by connecting many power semiconductor devices, i.e., Insulated Gate Bipolar Transistors (IGBTs) in cascaded mode with distinct DC sources. Because all DC sources in a symmetrical MLI topology are equivalent to  $V_{dc}$ , we consider existing MLI to be a symmetrical topology. For a seven-level cascaded MLI is made up of three H-bridges and three voltage sources. Every switch in the topology necessitates the use of a gate driver circuit. The number of inverter levels is determined by the switches utilised. A total of 12 switches is employed in this architecture. Each H-bridge is powered by a single DC voltage source. Here output voltages are  $+3V_{dc}$ ,  $+2V_{dc}$ ,  $+V_{dc}$ ,  $0$ ,  $-V_{dc}$ ,  $-2V_{dc}$ ,  $-3V_{dc}$  [21]. The output voltage in terms of the H-bridges equation is given by

$$V_o = 2k + 1 \quad (1)$$

Where  $k$  is the number of H-bridges.

Number of output voltage levels in terms of a power semiconductor device [22]

$$V_o = \frac{m+2}{2} \quad (2)$$

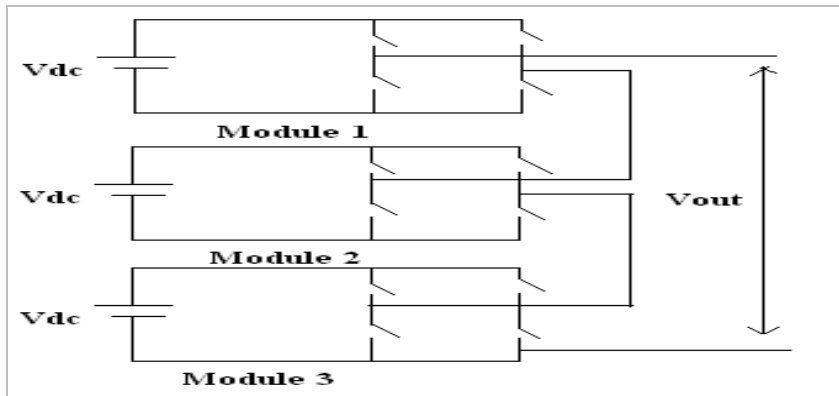
Where  $m$  denotes Power semiconductor devices. The *Figure 1* shows the conventional 7-Level CHB inverter.

*Figure 2* shows a block diagram of a reduced switch MLI using a PWM approach for grid-connected PV

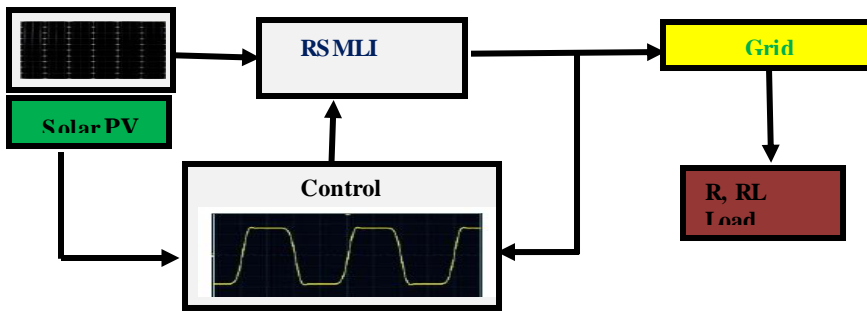
applications. The cascade multilevel inverter in this architecture is made up of nine IGBT switches and three DC Sources. Five of the nine switches are separate, with the remaining switches stacked in a cascade fashion to provide positive and negative polarities of output voltage. A higher number of voltage sources in a topology results in more steps in the output waveform, which improves the sinusoidal wave with a better harmonic spectrum, reduced power losses, and more accuracy at load.

**c) Modified 7-Level CHB-MLI with reduced switches**

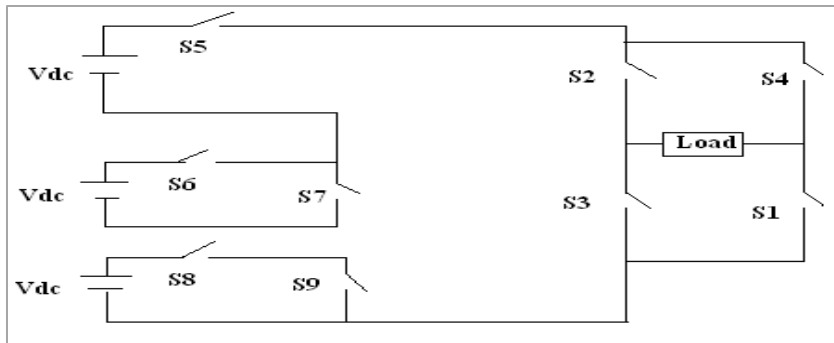
The greatest output voltage that the 7-Level Inverter can generate is  $3V_{dc}$ , and switches S5, S6, and S8 are all turned on. Similarly, the ON State status of switches at different levels is illustrated in *Table 1*. Every switch in a topology necessitates the use of a gate driver circuit [23]. *Figure 3* depicts the proposed cascaded MLI architecture, which comprises of nine switches. In contrast, a traditional cascade contains 12 switches. By comparing these two topologies, three switches are removed from the standard cascade MLI, resulting in a reduction in circuit complexity and total cost of the equipment module.



**Figure 1** Conventional Seven level CHB inverter



**Figure 2** RSMLI with PWM control



**Figure 3** Modified seven level Inverter

**Table 1** Switching states of reduced 7-level inverter

Switches/switching state					Output voltage (Volts)
S5	S6	S7	S8	S9	
1	0	1	0	1	Vdc
1	1	0	0	1	2Vdc
1	1	0	1	0	3Vdc
0	0	0	0	0	0
0	1	0	1	0	-Vdc
0	0	1	1	0	-2Vdc
0	0	1	0	1	-3Vdc

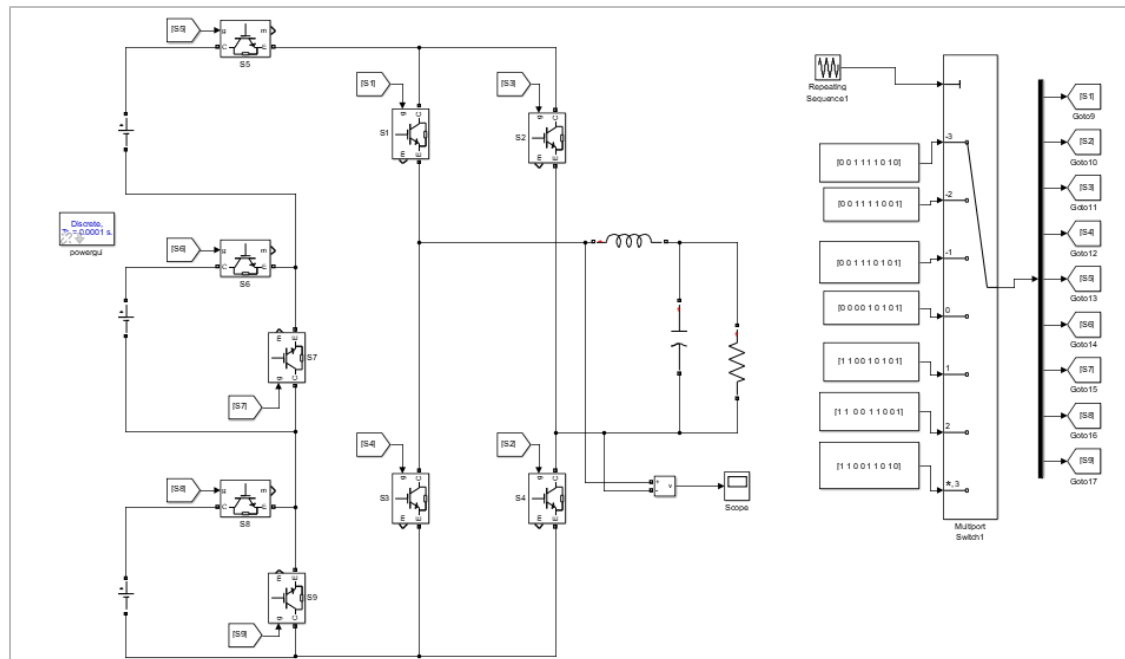
**4.Phase opposition disposition technique**

Switches in an inverter change positions between two states to regulate the output voltage (i.e., ON, OFF). This procedure is repeated indefinitely by varying the width of the pulses [24]. The POD technique is used in this topology. It is a carrier-based modulation technique used to generate pulses for the proposed cascaded seven-level inverter. Carrier waveforms above the reference are in phase in the phase opposition disposition technique, whereas those below zero are 180 degrees out of phase. CHB-MLI needed six carrier waveforms for seven levels, which are comparable to the modulating sinusoidal signal of 50 Hz waveform [25]. The positive and negative polarity of pulses is created, and these pulses form the switching sequence of the inverter to get the required

output voltage. The number of carrier waveforms (T) equals N-1, where N is the number of levels.

**5.Simulink models**

Figure 4 depicts a seven-level CHB-MLI constructed with nine IGBT switches. It has three DC voltage sources and a load resistance range of 10V and 10Ω. An LC-filter is attached to the Inverter output to reduce harmonics at the load end. For this topology, pulses are created using the POD approach, which compares six carrier waves with a frequency of 5 kHz to modulated sinusoidal signals with a frequency of 50 Hz. Figure 5 shows the Simulink model of unequal pulse width technique. Figure 6 shows the Simulink model of phase opposition disposition method (Ma=1, Ma<1).



**Figure 4** Simulink model of equal pulse width technique

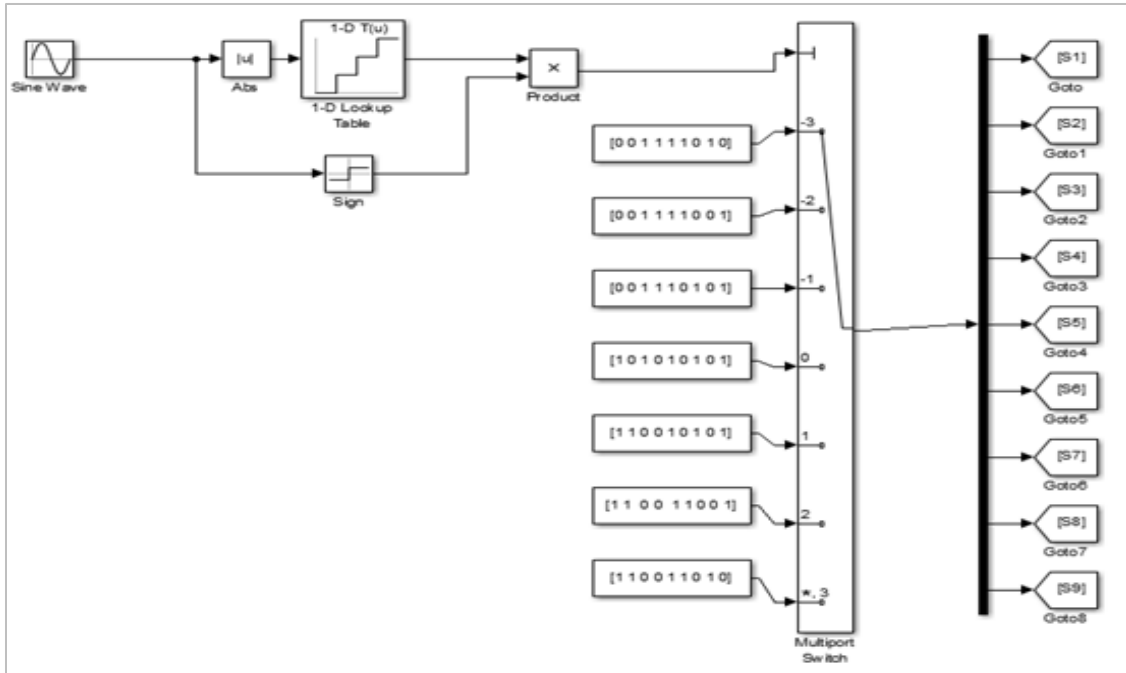


Figure 5 Simulink model of unequal pulse width technique

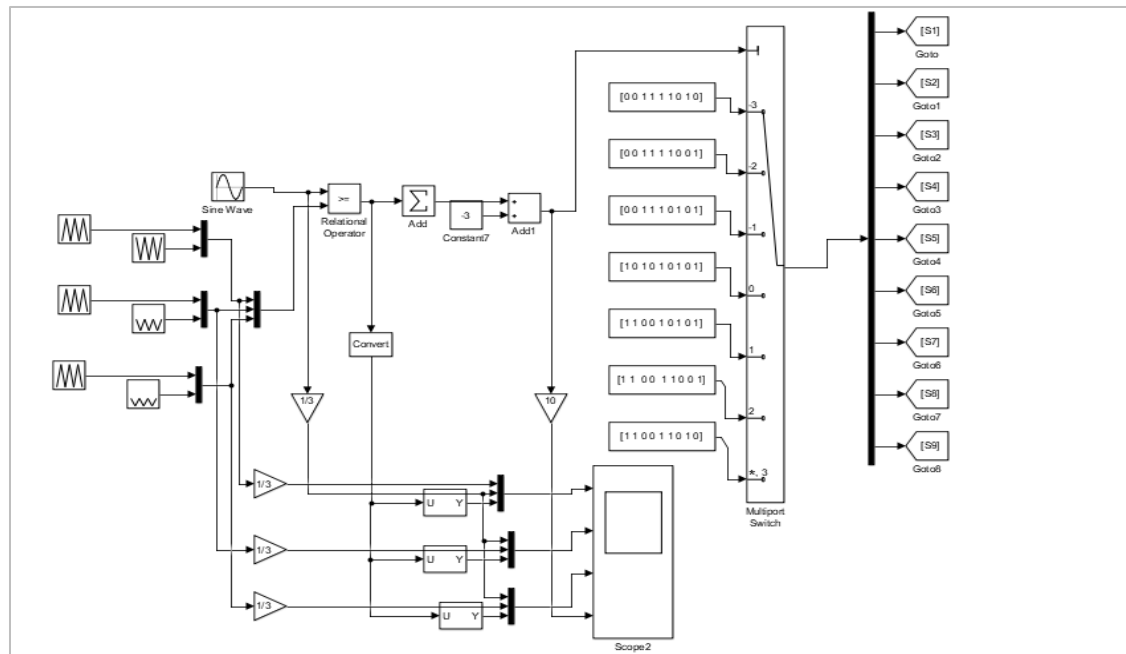


Figure 6 Simulink model of phase opposition disposition method ( $M_a=1$ ,  $M_a<1$ )

## 6.Results

Figure 7 depicts the output THD of a conventional 7-level inverter, whereas Figure 8 depicts the THD with reduced switch MLI caused by an uneven voltage source. PWM pulses are created by comparing a triangle wave to a fixed sinusoidal wave [26]. When

compared to uneven PWM, equal pulse width has a larger level of THD. Figure 9 shows the Fast Fourier Transform (FFT) Analysis of unequal pulse width technique. In uneven pulse width modulation, third order harmonics are missing. Figure 10 depicts the output voltages of the Phase opposition disposition

approach when the modulation index ( $M_a=1$ ) is used. Pulse produced by comparing six triangular carrier waves at 5 kHz to a fixed sinusoidal wave at 50 kHz. When the modulation index is equal to one using the multi carrier POD technique, higher order harmonics are created than before. *Figure 11* depicts the outcome of the phase opposition disposition approach using modulation index ( $M_a<1$ ), indicating that higher order

harmonics are significantly decreased. *Figure 12* shows the FFT analysis of phase opposition disposition technique ( $M_a<1$ ). *Figure 13* shows the FFT analysis of POD technique with filter ( $L=10\text{mH}$  and  $C=100\mu\text{F}$ ). Because the proportion of higher order harmonics is significant, LC filters are required for a modulation index of one.

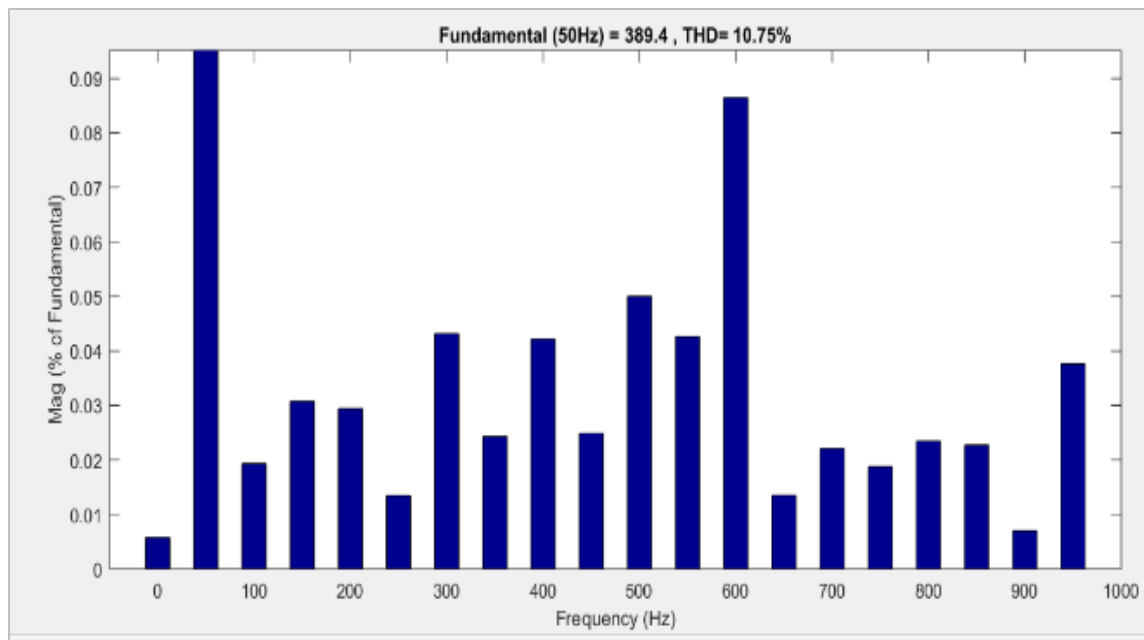


Figure 7 Conventional 7-level inverters: FFT analysis

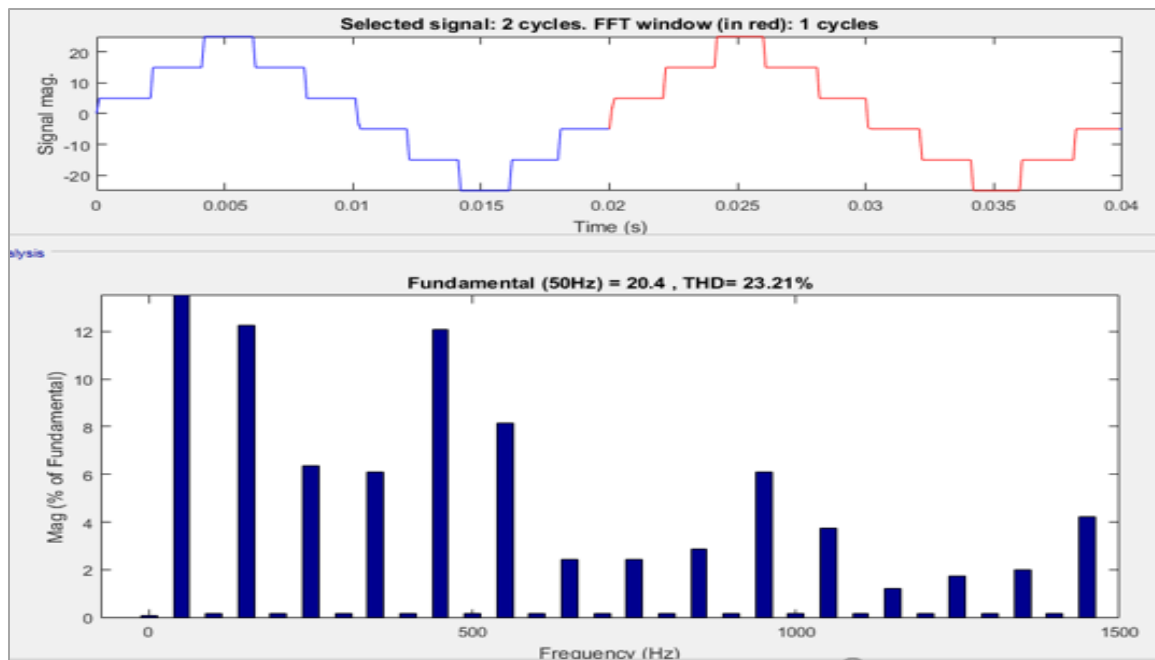


Figure 8 FFT Analysis of equal pulse width technique

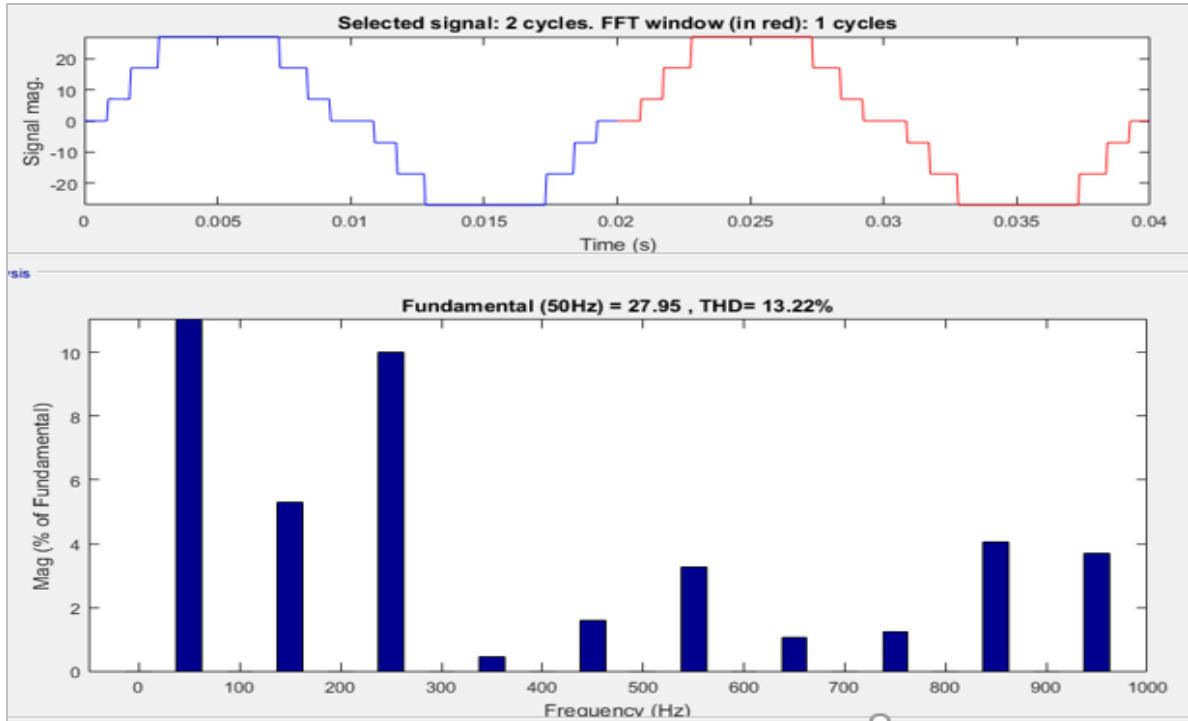


Figure 9 FFT Analysis of unequal pulse width technique

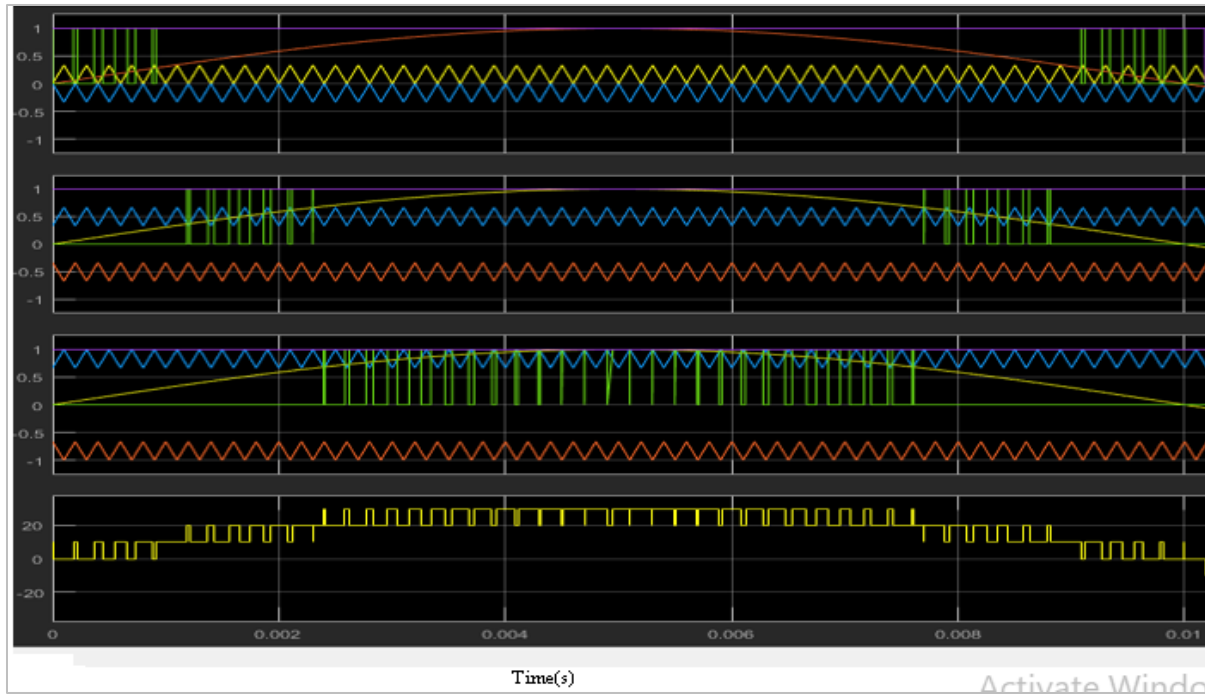


Figure 10 Output of POD multicarrier technique



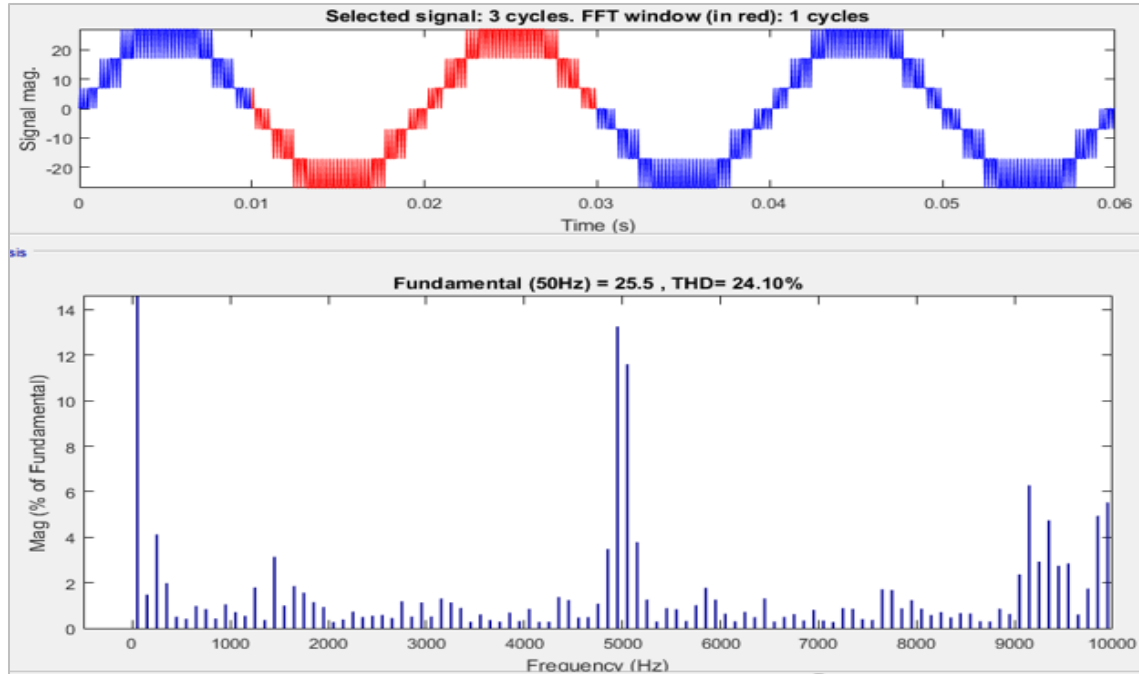


Figure 11 FFT Analysis of phase opposition disposition technique (Ma=1)

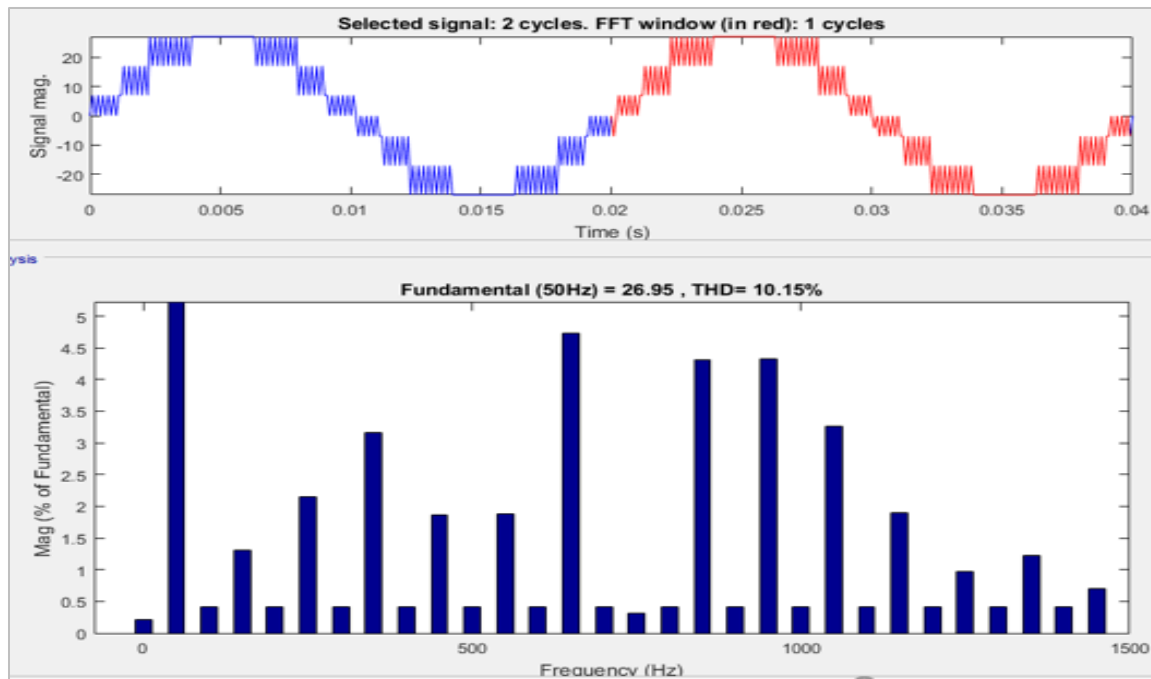


Figure 12 FFT analysis of phase opposition disposition technique (Ma<1)

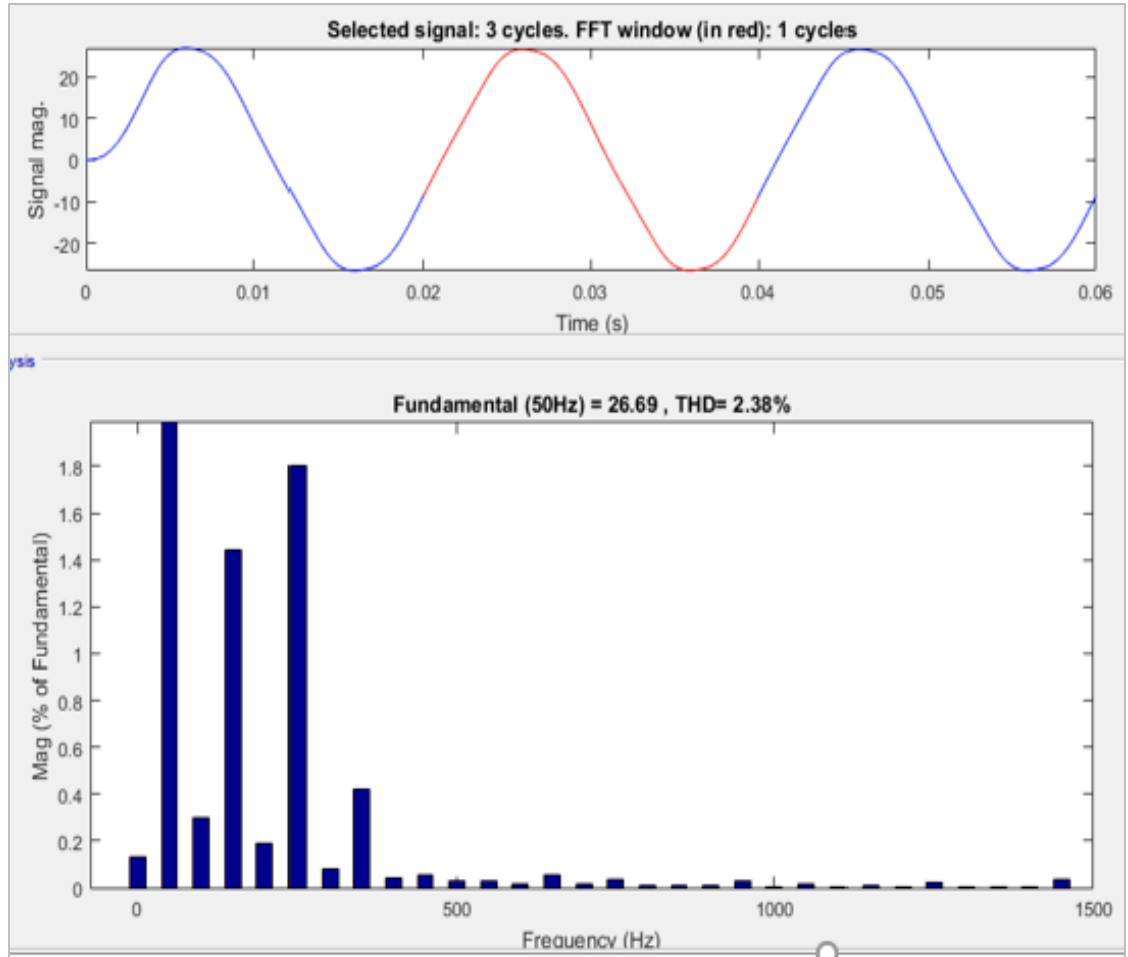


Figure 13 FFT analysis of POD technique with filter (L=10mH and C=100uF)

### 7.Data analysis and discussions

Table 2 compares different characteristics. In a capacitor clamped inverter, 14 capacitors and 10 switches are needed, but a diode clamped inverter requires 6 capacitors, 8 diodes, and 10 switches. The suggested RSMLI architecture reduces the number of switches to 9 and eliminates the need for capacitors and diodes. RSMLI architecture not only minimises the number of switches, but also the circuit complexity. Despite various benefits, the RSMLI

suffers from voltage stress on switching devices, since the decrease in switches increases voltage stress on switching devices. This voltage stress issue may be avoided by adopting higher switch ratings that can endure voltage stress. Table 3 compares THD with and without filter, with a same pulse width with filter the THD value is 13.04% and without filter it is 23.21%. The POD technique is used to analyse three modulation index values: (Ma=1), (Ma<1) the associated THD values are 24.11%, 10.15%, and 2.38%, respectively.

Table 2 Comparison of various parameters

Parameter	Capacitor clamped	Diode clamped	Conventional cascaded H-bridge	Proposed topology
No.of Capacitors	14	6	---	--
No.of diodes	--	>8	---	--
No. of switches	10	10	12	9

**Table 3** Comparison of total harmonic distortion

Sl. No.	Parameter	Total Harmonic distortion (THD)		No. of H-bridges and DC sources
		Without filter	With filter	
1	Conventional 7-level Inverter	10.75%	NA	3
2	Equal pulse width technique	23.21%	13.04%	3
3	Unequal pulse width technique	13.2%	6.44%	3
4	Phase opposition disposition technique (Ma=1)	24.11%	2.38%	3
5	Phase opposition disposition technique (Ma<1)	10.15%	1.89%	3

## 8. Conclusion

The seven-level CHB-MLI topology with fewer switches is modelled in a Simulink-MATLAB environment using the Phase opposition disposition approach and the suggested topology's functioning with equal and unequal pulses is investigated. The simulation results show that a modulation index of less than one ( $M_a < 1$ ) gives the appropriate seven-level output wave with a low THD percentage. THD was found to be 10.15% without a filter and 1.89% with one.

Future suggestions are as follows:

- The topology may be expanded further by creating a good control design using an improved methodology that takes into account the voltage stress on semiconductor devices.
- By keeping an eye on the voltage stress on the switching devices, the switch count may be lowered.
- With small adjustments to grid side parameters, this architecture might be used for active, reactive power control in grid-tied solar systems.

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## Conflicts of interest

The authors have no conflicts of interest to declare.

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