

Electronic combination lock system using verilog HDL

Nadia Mohamad Nasir¹, Irni Hamiza Hamzah^{2*}, Azman Ab Malik¹, Mohd Hanapiah Abdullah¹, Alhan Farhanah Abd Rahim¹ and Ahmad Asri ABD Samat¹

Faculty of Electrical Engineering, Universiti Teknologi MARA, Cawangan Pulau Pinang, Malaysia¹

School of Engineering, Penang Skills Development Centre, Penang, Malaysia²

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Abstract

Recently, burglary and robbery cases has been increasing and one of the factors that contributes to the growth of these cases is the weakness on the old-style home security system. The old-fashioned key and lock system may bring challenges to the effectiveness of the system since the keys are exposed to the risks of being lost and duplicated. The advancement of technology has introduced an electronic combination lock system in which only the house owner and selected people can unlock the doors. A main goal of this paper is to design and develop an electronic combination lock system using Verilog code. The entrance door of a house will only unlock if the user slides the correct secret code on the slide switches of the Altera DE2-115 Trainer Board. A Verilog code of the keyless system had been designed and scripted in Intel Quartus Prime Software. The simulations via testbench waveforms are performed in ModelSim Software. When the system detected the entered code matched with the setting code, the door is going to unlock. Besides, when the system detected the entered code did not match the setting code, the door is still unlocked. When the user entered correct password, all green LEDs turned on and the LCD displayed "Welcome Home". Besides, when the user entered an incorrect password, all red LEDs turned on and the LCD displayed "Wrong Password". The output displayed are successfully demonstrated on the Altera DE2-115 Trainer Board according to the desired results.

Keywords

Home security system, Keyless lock system, Field programmable gate arrays (FPGA), Hardware description language (HDL).

1.Introduction

A study made by Wei et. al had agreed that the old-fashioned key and lock system may brought challenges to the effectiveness of the system since the keys are exposed to the risks of being lost and duplicated [1]. This feature is believed to be insecure as break-in can easily occur when the keys were duplicated [2]. The statistical analyses found that a house without a security system is more frequent to be broken-in compared to the houses that had been well-equipped with security features [3]. Normally, when an event such as intrusion occur, it presents itself arbitrarily, and there might be noticeable physical evidence is witnessed of their occurrence when completed or they pass without notice based on the purpose of the intruder [4].

Therefore, this project was being inspired by the project conducted by Yeap [2] on designing the keyless lock system and continued the project to the hardware implementation. The main objective of the project proposed here is to design and develop an electronic combination lock system in order to improve the security features of a house. Nowadays, with the urbanization and miscellaneous criminal types, the efficiency of the key-and-lock has been challenged [5].

This keyless lock system is a security feature which only allows the house owner to unlock the door by sliding the secret code on the slide switches available on the Altera DE2-115 Trainer Board. The entry of the secret code was being designed by creating the code and the code length variable. For example, the secret code consists of four-digit numbers. Therefore, the house owner necessarily needed to know the accurate secret code and the code length. In order to unlock the door, the owner of the house had to insert

* Author for correspondence

a combination of the secret code on the slide switches. The door will be unlocked only when the code entered by the house owner is compatible with the setting code. Besides, the keyless lock system will activate the sleep circuit after entering invalid password for three consecutive times to indicate that the system is in a pending mode.

2.Literature review

The idea of the keyless lock system proposed in this project was almost similar with the project of the application of the Field Programmable Gate Arrays (FPGA) on a smart home security system conducted by Saleh et al. [6]. A smart home system designed by Saleh et al. emphasized several security features such as digital entry for automatic lock entrances and security sensors to sense the uneven movement or uncertain temperature. Both projects used the same hardware design which is Altera DE2-115 Trainer Board in order to process the password entered by the user and display of the entry status. The project designed by Saleh et al. used pushbuttons available on the Altera DE2-115 Trainer Board as the entry controller to unlock the doors. However, instead of using the pushbuttons on the FPGA as in [6], this project is going to use slide switches which were also the features available on the Altera DE2-115 Board itself. This project focused on implementing the hardware design of the lock system rather than the security sensors as designed by Saleh et. al Besides, this project extended from the project on the keyless coded home lock system [2]. The project conducted by Yeap et al. [2] only focused on the system design.

2.1Home security system

Ha [7] in his study also agreed that a burglar usually tried to penetrate a private area such as a house by dodging the door lock. Based on Anitha [8] 58% of the burglary's cases reported in USA are the aggressive break-in cases because a burglar only needs 8 to 12 minutes to break in an entry. Thus, smart home security control system has become crucial in everyday life [9].

2.2Field programmable gate arrays (FPGA)

FPGA have started to take its place in new applications with their high-performance features for parallel computing and signal processing [10, 11]. The biggest advantage of using the FPGA device as a new component in the industrial environment is that the different hardware features of FPGA (flexible and reusable integrated circuit, computing parallel tasks, cost efficiency, multiple input/output capability etc.) that can be designed by a developer for different

application platforms after production [12, 13]. FPGA can provide a wide opportunity for modern applications [14]. Besides, FPGA provides an impacted size and low power consumption solution [15]. FPGAs use dedicated hardware for processing logic and do not have an operating system. On the other hand, FPGA is very suitable for time-critical systems applications because every task on the FPGA hardware can utilize a different set of logic to be simultaneously run [16, 17]. Based on a study by Rodríguez-Andina et al. [18], FPGA is one the preferred implementation platform in many industrial applications because it can support high-speed, short time-to-market, good cost-performance and availability of specialized intellectual property (IP). The FPGA is able to be programmed over two ways: straightforwardly starting with An PC utilizing the around board stage flash ROM or through the USB port [19]. A "smart home" technology is one realization of home automation ideals that employs the integrated digital systems such as FPGAs technology [6].

2.3Hardware description language (HDL)

HDL may help the engineers to design a circuit logically and also functionally thus they can simulate and calculate accurately the performance of the circuit [20]. HDL is a computer-based language that had been widely used in order to describe the structure and behaviour of electronic circuits and digital logic circuits. One of the benefits of using HDL to simulate digital processing of any logical inputs is because the immediate FPGA based hardware implementation [21]. It looks like the common computer programming such as the C language, however HDL is specifically used to describe the structures of a hardware and the behaviour of logic circuits. In public domain, there are two standard HDLs that are supported by IEEE which were VHDL and Verilog. As for this project, the keyless lock system is being designed using Verilog coding. Verilog coding can support the logic control for production and the specification of the hardware circuitry as well as simulation and testing [22].

3.Methods

This project was divided into two parts which were simulation via testbench waveform and hardware implementation. There are two types of computer software used in this project which were Intel Quartus Prime Software and ModelSim Software. A hardware device used in this project is Altera DE2-115 Trainer Board.

3.1 Design simulation process

A Verilog code of a keyless lock system is being designed and developed in Intel Quartus Prime Software. A testbench coding is required in order to simulate the designed Verilog code of the keyless lock system. The purpose of simulation is to do functional verification as well as to implement the required system behavioural correctly. The simulation part will take place in ModelSim Software, a simulator developed by Mentor Graphics that offers a simulation environment to simulate HDL designs. The results of the simulation were in the form of testbench waveforms.

3.2 Design entry

```

module LockSystem(
  input CLOCK_50,      // 50 MHz clock
  input [17:0] SW,     // Slide Switches
  output reg [8:0] LED_GREEN, // GREEN LED
  output reg [17:0] LED_RED, // RED LED

  // LCD Module 16X2
  output LCD_ON, // LCD Power ON/OFF
  output LCD_BLON, // LCD Back Light ON/OFF
  output LCD_RW, // LCD Read/Write Select, 0=Write, 1=Read
  output LCD_EN, // LCD Enable
  output LCD_RS, // LCD Command/Data Select, 0=Command, 1=Data
  inout [7:0] LCD_DATA // LCD Data bus 8 bits
);

```

Figure 1 Example of verilog code

```

LCD_Display u1(
  // Host Side
  .iCLK_50MHZ (CLOCK_50) ,
  .iRST_N (DLY_RST) ,
  .SW (SW) ,

  // LCD Side
  .DATA_BUS (LCD_DATA) ,
  .LCD_RW (LCD_RW) ,
  .LCD_E (LCD_EN) ,
  .LCD_RS (LCD_RS)

```

Figure 2 Instantiating process to connect two different modules

3.3 Hardware implementation

Once the Verilog code is being verified in the ModelSim software, then only the Verilog code can be implemented on the Altera DE2-115 Trainer Board.

3.4 Pin assignments

Figure 3 shows the example of assigning the pin location. All the parameters declared in the Verilog code needed to be assigned correctly to avoid any unworking pins on the Altera DE2-115 Trainer Board. This step will automatically save as “.csv” file which is known as Comma Separated Value file. Therefore, the users do not to assign the pins again if they wish to run the project later on. Then, a “.sof”

file will be downloaded to the Altera DE2-115 Trainer Board using In System Memory Content Editor tools. This file is a binary file produced by the Compiler’s Assembler module containing the data of the created Verilog code of the keyless lock system which will be used to configure the FPGA device in the next step.

Figure 1 shows that there are 18 bits for slide switches, 9 bits for green LEDs and 18 bits for red LEDs. Input and bidirectional ports are always wires while output ports can be wire or reg. The inputs for this keyless lock system are clock and slide switches while the outputs of this system are green LEDs, red LEDs and LCD display. There are two modules used in this system which are LockSystem module and LCD_Display module. Figure 2 shows the process of instantiating parameters to connect LCD_Display module in LockSystem module.

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3.5 Programming and configuring FPGA device

In order to implement the designed Verilog code of the keyless lock system, the FPGA device needed to be programmed and configured. The RUN/PROG switch is set to RUN position to run this step. Ensure that the mode selected is in JTAG mode. Then, the .sof file created from the previous step is being

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selected. Once the START button is clicked, the configuration data will be successfully downloaded if

all LEDs on the board lighted up and the progress status showed “100% (Successful)”.

	Node Name	Direction	Location
in	CLOCK_50	Input	PIN_Y2
in	KEY[3]	Input	PIN_R24
in	KEY[2]	Input	PIN_N21
in	KEY[1]	Input	PIN_M21
in	KEY[0]	Input	PIN_M23
out	LCD_BLON	Output	PIN_L6
io	LCD_DATA[7]	Bidir	PIN_M5

Figure 3 Examples of assigning locations of the pins

4. Results

Figure 4 shows the flowchart of the keyless lock system. In order to unlock the door, the user need to enter the secret code on the slide switch on the Altera DE2-115 Trainer Board. The system will then compare the entered code with the setting code. If the entered code match with the setting code, it will proceed to the next stage which is comparing the code length of the entered code with the code length of the setting code. If the code length of the entered code matched with the code length of the setting code, the door will be unlocked. Otherwise, the attempt counter will be increased by 1 and the system will restart to allow the user to enter a new code for the second time. On the other hand, if the code length of the code entered by the user do match with the code length of the setting code, the system will start to count the number of unsuccessful attempts. If the number of unsuccessful attempts had reached more than three attempts, the system will automatically sleep. However, if the number of the unsuccessful attempts did not reach three times, the system will be reset to allow the user to enter a new code. Thus, the objective on this paper that is to introduce an electronic combination lock system to replace the old-fashioned key and lock security system had been achieved.

4.1 Testbench modelsim

The Verilog code of the keyless lock system is compiled and simulated in ModelSim Software. For the testbench, all the inputs and outputs have been declared in the UUT which is known as Unit Under Test [23]. This UUT needs to be instantiate in designing a testbench. This UUT acts as port mapping method which shows the connections of outputs and inputs from the main operation of

Verilog [24]. Three testbench codes were being developed to perform the functional verification on the designed Verilog code. The first testbench is to test the keyless lock system when the code entered by the user matched with the setting code while as for the second testbench is to test the designed the Verilog code when the user enter an invalid password. On the other hand, the third testbench displayed the output waveform when the user input invalid password for three consecutive attempts.

Figure 5 shows the output waveforms keyless lock system when the code entered by the user is correct. The setting code for this keyless lock system is ‘1001’. Once the system detected the user entered ‘1001’, the system will start to compare the code length of the entered code and the setting code. When the code length of both codes matched each other, the code length waveform goes logic ‘1’. UNLK waveform goes high to indicate that the door is going to be unlocked. Then, logic 1 in the clear_unsuccessful will clear the number of unsuccessful attempt whereas logic 1 in clear_reset will reset the keypad pointer back to 1 respectively.

Figure 6 shows the output waveform of the keyless lock system when the user entered an invalid password. When the user entered ‘1101’, the system detected that the entered code is not equivalent with the setting code. Therefore, the UNLK waveform is not activated indicating the door is not going to unlock. Besides, the clear_unsuccessful and clear_reset are also inactivated.

Figure 7 shows the output waveform of the keyless lock system when the user input invalid password for three consecutive times. For the first incorrect

attempts, unsuccessful_attempt1 goes high and the second incorrect attempts will then trigger the unsuccessful_attempt2 to activate. When the user input the third incorrect password, the unsuccessful_attempt3 will go to logic '1'. On the other hand, the UNLK will not activate to signify that the door is still locked. This will activate the sleep_circuit and the whole system will be in pending mode for 3 minutes. Therefore, the

clear_unsuccessful and clear_reset will remain logic '0' showing the system is in sleep mode. Table 1 shows the tabulated logic of the parameters obtained in the testbench waveforms for the three different situations. Case 1 is for entering a valid password, case 2 is for entering an invalid password and case 3 is for entering invalid password for three times.

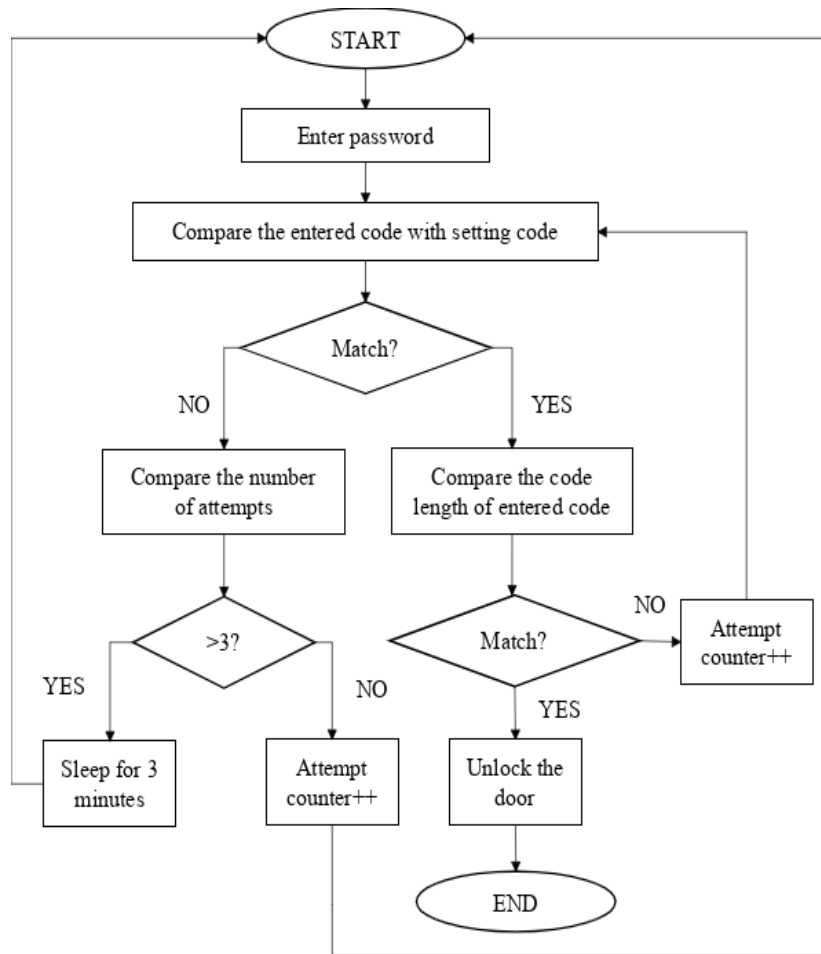


Figure 4 The flowchart of the keyless lock system



Figure 5 Output waveforms of the keyless lock system when the code entered is valid

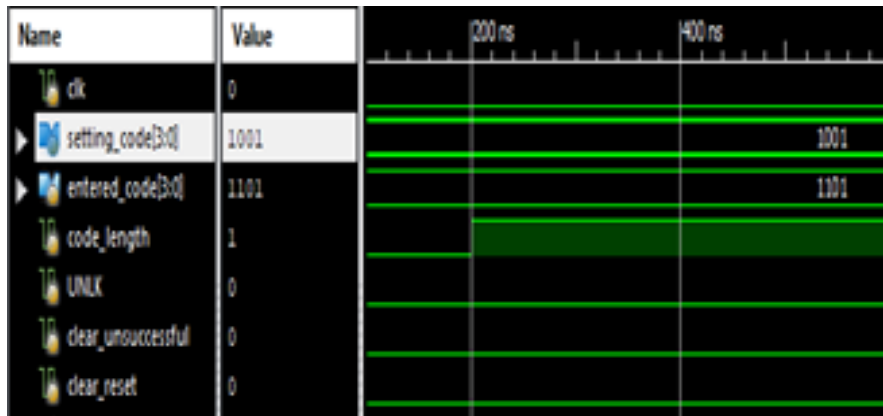


Figure 6 Output waveforms of the keyless lock system when the code entered is invalid

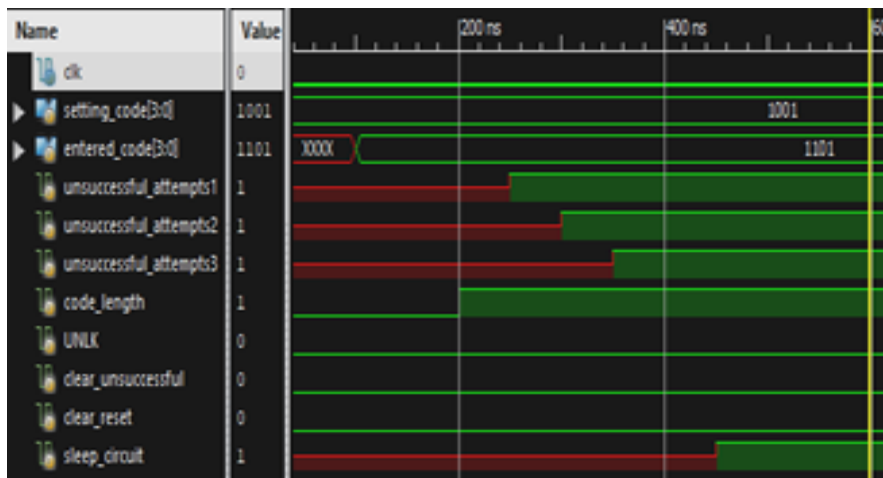


Figure 7 Output waveforms of the keyless lock system after 3 unsuccessful attempts

Table 1 The logic table of output waveforms for three different situations

Case	Setting code	Entered code	Code length	UNLK	clear_unsuccessful	clear_reset
1	1001	1001	1	1	1	1
2	1001	1101	1	0	0	0
3	1001	1101	1	0	0	0

4.2 Hardware implementation

The inputs for this system are slide switches while the outputs of the system are the green LEDs, red LEDs and LCD display. The system begins with an initial output on the LCD display which displayed “SMART HOME” on the first line while “Enter Password” on the second line as shown in Figure 8.

In order to unlock the door, the user needs to input the password on the slide switches. The setting code that had been set for this keyless lock system is 1001.

Once the inputs entered by the user matched with the setting code set in the Verilog code, all the green LEDs will be turned on and “Welcome Home” will be displayed on the LCD display as shown in Figure 9.

On the other hand, when the system detected that the user inputs an incorrect password on the slide switches, all red LEDs will turn on. A “Wrong Password” will be displayed on the LCD display as shown in Figure 10.

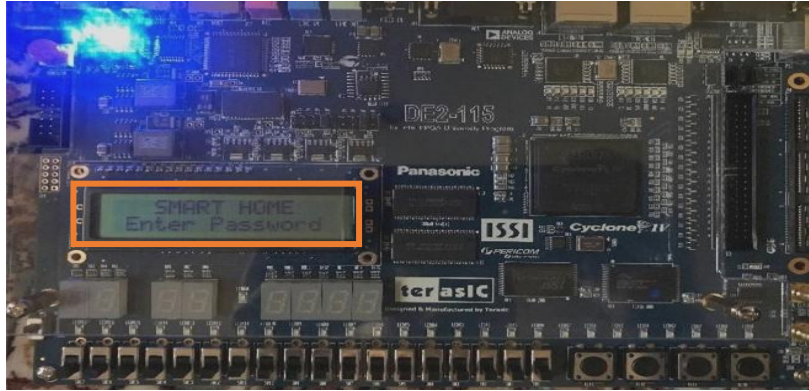


Figure 8 The initial display of the system

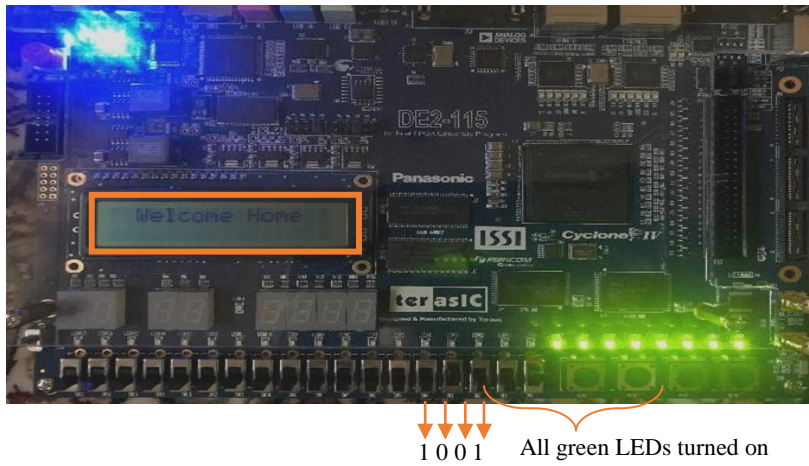


Figure 9 All green LEDs turned on

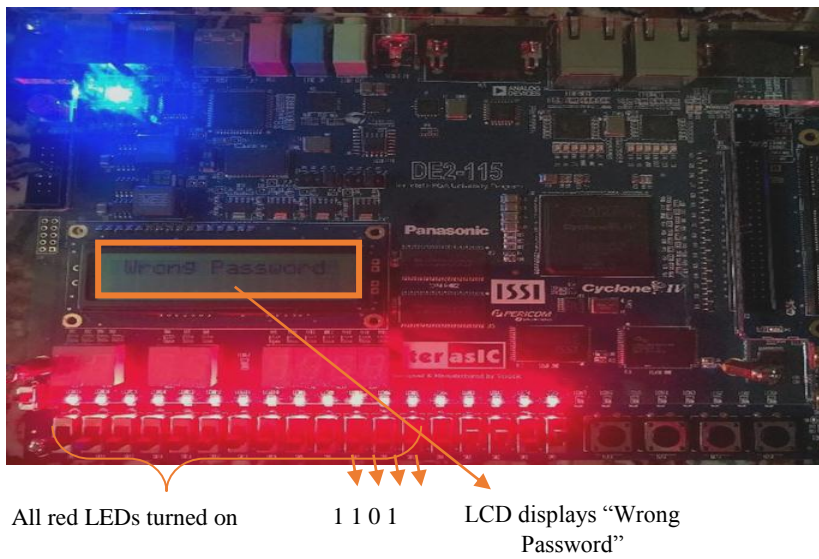


Figure 10 All red LEDs turned on

5. Discussion

The study conducted by Yeap [2] also designed three different types of testbench codes for design verification. The first testbench is when the code entered by the user is correct and the second testbench is when the user entered a wrong password. The third testbench shows the output waveforms after 4 unsuccessful attempts. The first and second testbench were almost similar with the project proposed in this paper. However, the system flows of both projects were slightly different. The keyless coded home lock system designed by Yeap [2] comprises five different modules which were setup panel module, code checker module, keypad and encoder module, control unit module and sleep circuit module. Meanwhile, the electronic combination lock system designed in this paper only comprises of two modules which were lock system module and decision-making module which was the UNLK module. Most of the process of checking code, checking code length, calculating number of attempts, and sleep circuit occurred in one module only which was the lock system module. This make the keyless lock system introduced in this paper to be simpler as it may reduce the time taken to make the decision in unlocking the door.

In contradict with the electronic combination lock system proposed in this project, once the system detected that the entered code did not match with the setting code as shown in Figure 7, the whole system will stop processing immediately. The UNLK waveform will directly inactivate indicating the door was not going to unlock instead of checking the code length of the entered code as designed by Yeap [2]. Inactivation in the UNLK waveform will trigger the clear_unsuccessful and clear_reset to be inactivated. As opposed to the electronic combination lock system in which there was no reset button designed for the user to reset the system. Therefore, after the lock system detected the third unsuccessful attempt, the UNLK will automatically not activate to signify that the door is still locked. This will trigger the sleep_circuit and the whole system will be in pending mode for 3 minutes. Therefore, the clear_unsuccessful and clear_reset will remain logic '0' showing the system is in sleep mode.

A smart home system designed by Saleh et. al emphasized several security features such as digital entry for automatic lock entrances and security sensors to sense the uneven movement or uncertain temperature. The project constructed by Saleh et al. [6] used Altera DE2-115 board to process the signal

transmitted from temperature sensor to FPGA board and which will then display the entry status after entering the password and activation security system on the LED seven segments displays. The entry login controller will use a push button or switches available on the FPGA board that are used to login password for the automatic doors. The electronic combination lock system designed in this paper also used the Altera DE2-115 Trainer Board in order to process the password entered by the user and display of the entry status. The project designed by Saleh et al. [6] used pushbuttons available on the Altera DE2-115 Trainer Board as the entry controller to unlock the doors. However, instead of using the pushbuttons on the FPGA, this project use slide switches which were also the features available on the Altera DE2-115 Board itself. By using slide switches, the interface will be more user-friendly as the user only need to slide the switches instead of the need to long-press the pushbuttons. Besides, this project focused on implementing the hardware design of the lock system rather than the security sensors as designed by Saleh et al. [6].

6. Conclusion and future work

In conclusion, an electronic combination lock system had been successfully designed using Verilog code. The output waveforms of the system had been verified and presented in ModelSim software. The output results simulated are equivalent with the designed testbench codes. The Verilog code of the keyless lock system had been implemented on the Altera DE2-115 Trainer Board. For future work, it is recommended that this project can be extended to the sound of alarm after three wrong inputs were key-in. The sound of the alarm can alert the neighbourhood that the possibility of robbery occurred in their vicinity. Then, this warning can be link directly to the owner of the house via the handphone. Therefore, the alert and trigger system will be more effective in order to educate the community to help police decreased the number of reported crime cases.

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Conflicts of interest

The authors have no conflicts of interest to declare.

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Nadia Mohamad Nasir was born in Kuala Nerang on 19th February 1997. She obtained her B. Eng (Hons) in Electrical and Electronic Engineering in 2020, from School of Electrical Engineering, Universiti Teknologi MARA, Penang Branch Campus. She is currently a Graduate Trainee Engineer in Product Enablement Solution Group Department in Intel Microelectronics Sdn. Bhd. Her research interest is in Electronic Combination Lock System using Verilog

Coding. She is a registered Board of Engineers Malaysia (BEM) Professional Engineer.
Email: nadianaasir@gmail.com



Irni Hamiza Hamzah was born in Machang, Kelantan on 6th December 1974. She obtained her B. Eng (Hons) in Electrical and Electronic Engineering in 1998, MSc. Electronics System and Design Engineering in 2005 and PhD in BioMEMs Sensors in 2013, which all had been obtained from School of of Electrical and Electronic Engineering, Universiti Sains Malaysia, Malaysia. She is currently a Senior Lecturer in Electronic Engineering Department, Faculty of Electrical Engineering, Universiti Teknologi MARA, Penang Branch Campus, Malaysia. Her research interests include Biosensors, BioMEMs, Neural Networks and Renewable Energy. She is a registered Board of Engineers Malaysia (BEM) Professional Engineer.
Email: irnihami@uitm.edu.my



Azman Ab Malik was born in Melaka on 12 October 2018. He obtained his Diploma in Electronic Technology from KKTm Pasir Mas in 2007, Bachelor in Electrical Engineering and Technology from UNIKL BMI, Master in Electrical and Electronic Engineering from USM and Phd in Electrical Engineering from UiTM. His interest in innovation towards electrical and electronic and cross multi-disciplinary area to identify a new model or method in engineering. His research interest include Electrical Power, Power System, Renewable Energy, Hybrid System, Embedded System, Wireless Power Transfer and Energy Storage. He is currently a Senior Lecturer in School of Engineering, Penang Skill Development Centre, Pulau Pinang, Malaysia.
Email: azman@psdc.org.my



Ahmad Asri Abd Samat received a BSc. (Hons) Electrical and Electronic Engineering from MARA University of Technology, Malaysia and M. Eng (Electrical Energy and Power System from University of Malaya, Malaysia in 2004 and 2006, respectively. In 2019, he finished his PhD in the field of Electrical Machines and Drives from Universiti Sains Malaysia, Malaysia. Now, he is a Senior Lecturer in Electrical Engineering at the Faculty of Electrical Engineering, Universiti Teknologi MARA, Permatang Pauh Penang, Malaysia.
Email: hanapiah801@uitm.edu.my



Mohd Hanapiah Abdullah received a BSc. (Hons) Electrical and Electronic Engineering from MARA University of Technology, Malaysia and M. Sc (Microelectronics) in the field of Optoelectronics from University of UKM, Malaysia in 2000 and 2005, respectively. In 2015, he finished his PhD in the field of Nanotechnology Device Fabrication for Green Technology from UiTM, Shah Alam, Malaysia. Now, he is a Senior Lecturer in Electronic Engineering at the School of Electronics, Faculty of Electrical Engineering, Universiti Teknologi MARA, Permatang Pauh Penang, Malaysia. He is a member of the NanoElectronic Center (NET), Innovation Center (IOS), UiTM Shah Alam. He is looking forward to explore new area of research and collaborations with other parties.
Email: alhan570@uitm.edu.my



Alhan Farhanah Abd Rahim obtained her B.Eng Hons in Electronics Engineering from University of Southampton in 1998, MSc and PhD in Solid State Physics from Universiti Sains Malaysia in 2003 and 2014 respectively. She is currently senior lecturer at the Faculty of Electrical Engineering, Universiti Teknologi MARA, Malaysia. Her research interests are in synthesizing and fabricating advance semiconductor materials (group IV, III-V)) and devices utilizing low cost techniques. Her PhD research work entitle: Studies of Ge nanostructures Studies of Si and Ge Nanostructures Synthesized By Electrochemical and Plasma Assisted Techniques For Sensing Applications. She is author and co-author of over 20 scientific publications in this field. She is a companion member of Institute of Engineer's Malaysia (IEM) and a registered Board of Engineers Malaysia (BEM) Professional Engineer.
Email: ahmadasri759@uitm.edu.my