

## Efficient reconfigurable architecture for advanced orthogonal frequency division multiplexing (AOFDM) transmitter

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Received: 17-May-2018; Revised: 10-July-2018; Accepted: 12-July-2018

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### Abstract

The orthogonal frequency division multiplexing (OFDM) is most commonly used in the area of communication where a large amount of data needs to be transmitted through a wired or wireless channel. The main application OFDM lies in wireless network, internet model and digital video/audio broadcasting. Data need to be divided over a number of orthogonal channels to minimize the interference between each transmission channel and commonly performed using analog circuitry method. However, this method is less stable and bulky. In this paper, an efficient reconfigurable architecture for advanced OFDM transmission has been proposed. The architecture consists of 31 subcarrier channel, OFDM system using 64 point modified coordinate rotation digital computer (CORDIC) based inverse fast Fourier transform (IFFT) and novel 4 point quadrature amplitude modulation (QAM) is used for modulations of each channel. The input data is converted from serial to parallel, encoded using Hermitian symmetry, cyclic prefix, and converted serial to parallel. The comparison result shows that the proposed architecture is better than existing in terms of hardware utilizations. The proposed OFDM transmitter requires almost 35% lesser hardware resources with respect to existing techniques.

### Keywords

Inverse fast Fourier transform (IFFT), Quadrature amplitude modulation (QAM), Orthogonal frequency division multiplexing (OFDM), Transmitter, Cyclic prefix, FPGA implementation.

### 1. Introduction

The orthogonal frequency division modulation (OFDM) is used for communication purpose due to various advantages over other modulation techniques. Normally, OFDM technique divides the data flow to an orthogonal channel. This will minimize the interference occurring in the transmission between two or more signals carrying channel components. Insertion of noise to the signal by the modulation process is very less in case of OFDM. In large pass-band channel the noise model is unknown and unpredictable. To overcome this problem the total channel is subdivided into a number of sub channels which simplifies the noise calculation model. To implement this, the modulation scheme is subdivided into various different subcarrier frequencies in such a way that one channel does not intervene with other which preserve orthogonal property. An efficient reconfigurable architecture for an OFDM transmitter has been proposed in this paper.

The proposed architecture consists of serial to parallel conversion, encoder, Hermitman symmetry, IFFT and parallel to serial data conversion block. The main use of Fourier transform is to filter the frequency band effectively, which guards each interval frequency and to generate better modulation results.

The main objective of this paper is to design new hardware architecture for OFDM transmitter which consists of less hardware area than existing techniques. The contributions of this paper are summarised as (i) Novel state machine model is used to design QAM, and (ii) The IFFT is designed using modified CORDIC and Vedic multiplication technique to reduce hardware requirement.

### 2. Literature survey

Hwang et al. [1] proposed a detailed survey on OFDM and its corresponding applications on wireless system and also it describes the working of the general wireless communication system using the

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OFDM technique in details which includes various communication parameters such as channel estimation, signal detection, time and frequency offset estimation and full details needs to implement any OFDM system. Liu et al. [2] presents survey of existing techniques to estimate channels of an OFDM system. The author first surveys the channel frequency response (CFR) approach and then parametric model (PM) based approach and then compare with many newly invented approaches such as MIMO-OFDM and finally the authors conclude the best approach suitable for different conditions. Armstrong [3] presented a new technique to implement OFDM for optical communication. The author has used linear field modulation intensity modulation and MIMO technique for the implementation, but the result shows that for any optical OFDM linear field and intensity modulation techniques are more suitable than MIMO. Haque et al. [4] analyze a MIMO-OFDM for 4G system under Rayleigh fading. In any wireless system noise is a big issue which affects the performance of the system. In this paper the related parameters are greatly affected by noise and have modified the existing architecture to improve the performance. The presented technique shows better result in noisy condition than the existing. Perez-Calderon et al. [5] tried to enhance the time-frequency multiplexing using diversity technique. For this purpose related constellation (RC) technique is used. The proposed technique is compared with a frame of digital video broadcasting-second generation terrestrial (DVB-T2) standard. The result shows that the improvement of the proposed technique up to 1dB. Garcia and Cumplido [6] presented an efficient OFDM architecture which can be implemented on field-programmable gate array (FPGA). For this implementation, IEEE 802.16-2004 standards were considered. The architecture is designed on system generator software where some part of the architecture is coded using very high speed integrated circuit (VHSIC) hardware description language (VHDL) and the remaining parts are directly taken from the Simulink library for implementation. The authors used Virtex-2 FPGA to check the performance of the presented architecture. Chang and Sobelman [7] present pulsed OFDM system. The architecture is implemented on the Virtex-4 FPGA device and Simulink tool is used for design purpose. The main disadvantage is the requirement of large amounts of memory.

### 3.Basics of OFDM transmitter

An OFDM carrier signal is that the total of variety of orthogonal sub-carriers, with baseband information

on every sub-carrier being severally modulated usually victimization some form of quadrature amplitude multiplexing (QAM) or phase-shift keying (PSK).

This composite baseband signal is usually modulate a main RF carrier.  $S[n]$  may be a serial stream of binary digits. By inverse multiplexing, this square measure 1st de-multiplexed into  $N$  parallel streams, and every one mapped to (possibly complex) image stream victimization some modulation constellation (QAM, PSK, etc.). Note that the constellations are also totally different, therefore some streams might carry the next bit-rate than others. An inverse FFT is computed on every set of symbols, giving a collection of complicated time-domain samples. These sample square measures, then quadrature-mixed to pass band within the commonplace approach. The important and imagined elements square measure 1st regenerate to the analogue domain victimization digital-to-analogue converters (DACs); the analogue signals square measure then, to modulate cos and trigonometric function waves at the carrier frequency,  $f_c$  severally. These signals square measure, then summed to present the transmission signal  $s(t)$ .

The block diagram of the basic OFDM transmitter is given in *Figure 1*.

If  $N$  sub-carriers are used, and each sub-carrier is modulated using  $M$  alternative symbols, the OFDM symbol alphabet consists of  $M^N$  combined symbols. The low-pass equivalent OFDM signal is expressed as:

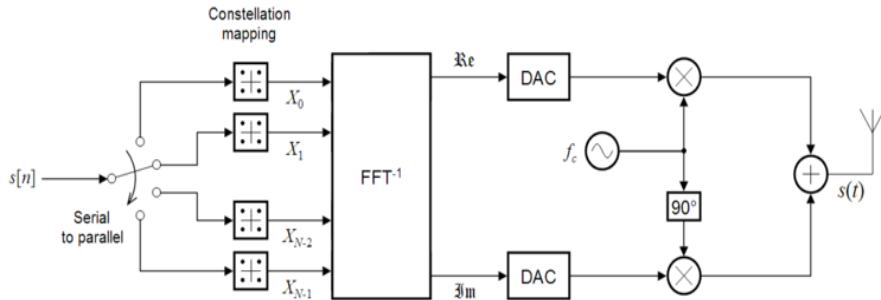
$$v(t) = \sum_{k=0}^{N-1} X_k e^{j\frac{2\pi k t}{T}}, \quad 0 \leq t < T \quad (1)$$

Where  $X_k$  are the data symbols,  $N$  is the number of sub-carriers, and  $T$  is the OFDM symbol time. The sub-carrier spacing of  $1/T$  makes them orthogonal over each symbol period; this property is expressed as

$$\frac{1}{T} \int_0^T e^{j\frac{2\pi(k_2 - k_1)t}{T}} dt \quad (2)$$

To avoid inter-symbol interference (ISI) in multipath fading channels, a guard interval of length  $T_g$  is inserted prior to the OFDM block. During this interval, a *cyclic prefix* is transmitted such that the signal in the interval  $-T_g \leq t < 0$  equals the signal in the interval  $(T - T_g) \leq t < T$ . The OFDM signal with cyclic prefix is thus

$$v(t) = \sum_{k=0}^{N-1} X_k e^{j\frac{2\pi k t}{T}}, \quad -T_g \leq t < T \quad (3)$$



**Figure 1** Basic OFDM transmitter

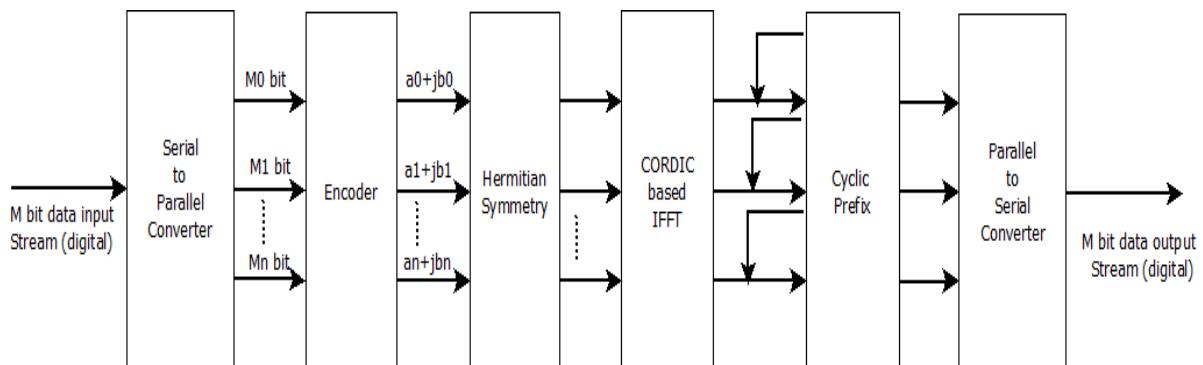
The low-pass signal above can be either real or complex-valued. Real-valued low-pass equivalent signals are typically transmitted at baseband-wire line applications such as digital subscriber lines (DSL) use this approach. For wireless applications, the low-pass signal is typically complex-valued; in which case, the transmitted signal is up-converted to a carrier frequency  $f_c$ . In general, the transmitted signal can be represented as:

$$s(t) = \sum_{k=0}^{N-1} |X_k| \cos\left(2\pi\left[f_c + \frac{k}{T}\right]t + \arg[X_k]\right) \quad (4)$$

#### 4. Proposed OFDM transmitter

The proposed architecture of OFDM transmitter is given in *Figure 2*. The architecture consists of serial

to parallel converter, encoder, Hermitian symmetry, cyclic prefix and parallel to serial converter block. The serial to parallel converter block converts the input data stream into a finite number of parallel data and are then encoded by encoder block into a finite number of data. The encoder is mainly constructed by 64 points QAM. The symmetric data present in the encoded data is removed by the Hermitian symmetry technique which is then fed to modify CORDIC based FFT block. This data is converted into cyclic code by using the cyclic prefix and send through channel serially through parallel to serial converter block.



**Figure 2** Proposed architecture for OFDM transmitter

#### 4.1 Serial to parallel converter and parallel to serial converter

The simple shift registers [8] are used to make these conversions.

##### 4.1.1 Serial to parallel converter

This is mainly used at the input side of any OFDM module. The main requirement of this block is to convert the serial data into a predefined number of parallel data. This is mainly opted through the uses of a predefined number of D flip-flops. The dimension of the flip-flop is directly equal to the number of channels required by the encoder.

With each rising edge clock, one bit is transferred from the input to the next flip-flop. This process will continue like a loop. The logical architecture for serial input and parallel output is shown in the *Figure 3*. Once the entire input sequence is present in the D flip-flop array the device start producing parallel output. This is the starting point of the valid output of the device. If we consider output generated before this point which is undefined value, then the architecture will generate the wrong sequence.

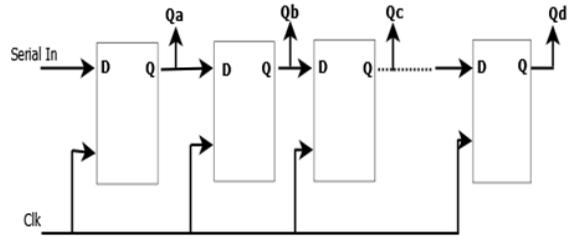


Figure 3 Serial input parallel output

#### 4.1.2 Parallel to serial converter

This is used at the output of the OFDM to serialize the calculated parallel sequence. This performs the reverse operation of the serial to parallel conversion. The operation of this block is similar to a commutator block present in any communication channel. To implement this we use an 8:1 MUX and a 3-bit counter as shown in *Figure 4*. The output of the counter is connected to the select line of the MUX. The counter count is incremented on each clock pulse which is used to select the line of the MUX. The counter counts are incremented on each clock pulse which is used to select different channel values which in turn makes the output synchronous to clock pulse which helps to synchronization purpose.

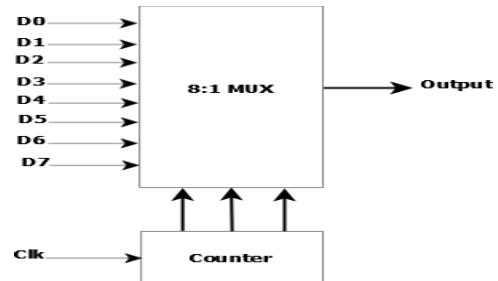


Figure 4 Parallel input serial output

#### 4.2 Encoder

The 'm' bit of the encoder of the encoder is converted into an  $a+jb$  format by the constellation maps used for the modulation purpose and is mainly used for suitable conversion of bits. This conversion is done by QAM. The input of the encoder is a binary number of m-bits. Whereas, the output consists of two binary numbers, one is in phase and another is in quadrature phase. The size of the output generated by this block is defined by IFFT block. The finite state machine (FSM) model for the encoder is given in *Figure 5*. For this purpose, we considered 4-point QAM.

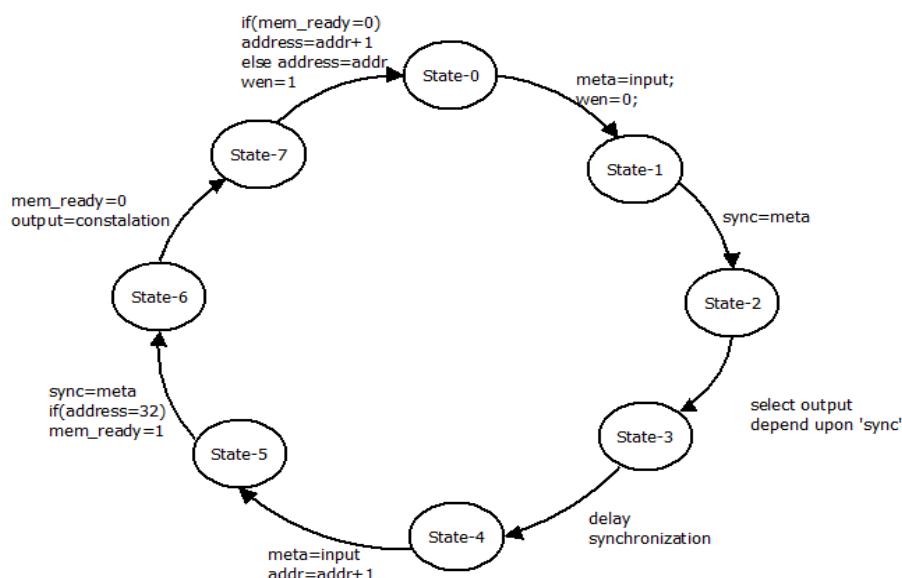


Figure 5 FSM model for proposed encoder

Quadrature modulation is a commonly used modulation scheme for both analog and digital signals. For our purpose, we consider QAM for digital bit stream of input signal. This scheme divides the input signal into two carrier waves of the same frequency component. Normally, each component is out of phase by 90° with each other signals. This

scheme is very efficient and used for various telecommunication operations.

In QAM constellation, all points are arranged in a sequential manner with having equal vertical and horizontal spacing. This is normally in terms of power of some integer number. By taking the higher point of QAM we can increase the compression ratio.

### 4.3 Hermitian symmetry

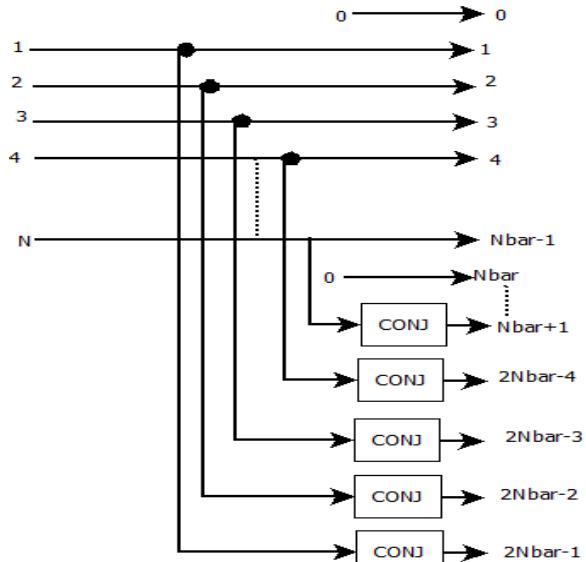
Normally a time domain signal of real valued is obtained by the Hermitian symmetry method. It is also known as discrete multitone (DMT) which is a special case of OFDM. This shows similar property of discrete Fourier transform (DFT) of any real valued signal. So, any real valued signal has Hermitian symmetry. For any low pass communication channel, the transmitted signal does not have any additional up-conversion, then proper communication the transmit signal must be real valued. Most of the cases before IFFT block, this block is used. To achieve this we have to map  $N/2$  complex symbols into subcarriers of range zero to  $(N/2-1)$  and then assign the respect complex conjugate value to the subcarrier. The equation of Hermitian symmetry [9] is given as

$$\begin{aligned} X_0 &= X_{\bar{N}} = 0 \\ X_k &= d_k \\ X_{2\bar{N}-k} &= d_k^* \end{aligned} \quad (5)$$

Where,  $d_k$ =Input at  $k^{\text{th}}$  location.

$X_N$ =Output at corresponding  $N^{\text{th}}$  location  
 $i=1, 2, \dots, (N-1)$ .

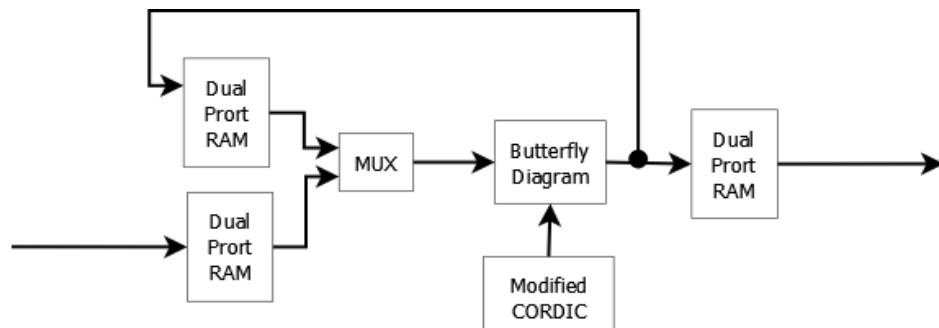
This is implemented by simply assigning opposite sign to the imaginary part of the signal as shown in *Figure 6*.



**Figure 6** Block diagram for proposed Hermitian symmetry calculator

### 4.4 CORDIC based IFFT

The inverse discrete Fourier transform (IDFT) equation is used to construct OFDM modulation for fast implementation with less hardware resources butterfly diagram is used. The block diagram of modified CORDIC [10, 11] based IFFT is given in *Figure 7*.



**Figure 7** Block diagram for proposed modified CORDIC based IFFT

To avoid overflow problems two extra bits are added to the block in the most significant bit side. In this implementation, we use 64 point IFFT where storing of all coefficients requires a large amount of memory which reduce the overall architecture operating frequency. To avoid this we store a minimum number of angles and calculate corresponding twiddle factors using modified CORDIC [10, 11] block.

The modulation OFDM may be created through an associate in nursing IDFT. The quick implementation of IDFT is IFFT which is used to reduce the time of

processing and also the used hardware. The reception, within the same method, may be created by DFT, or better, by FFT, that's it economical implementation. FFT calculates DFT with a good reduction within the quantity of operations, going away many existent redundancies within the direct calculation of DFT. The concept of FFT from DFT has made possible for high speed applications and also not compromise with the vital method of the quality procedure calculation. As a result, FFT is a particularly economical algorithmic rule that has an honest implementation in hardware for different

values of N. The total architecture in the butterfly possesses an equivalent algorithmic rule. To avoid overflow to total in complement of 2, it's created the extension of the sign up-to the binary variety, continuance the foremost vital bit, i.e., if it adds two binary numbers of ten bits, try and do the extension of the sign, to 2 numbers of eleven bits, This procedure has to be repeated each time which may add or to compute various data's. Already for the multiplication, the saturation existed when results in the total amount of bits of the 2 multiplicands. There in method, to try and do the multiplication of 2 numbers of ten bits. This procedure has got to be done to every multiplication. If there's not impediment, it may be created a rotation for right (divisions for two) within the numbers and to cut back its size, since within the end of the procedure a corresponding multiplier factor is applied. The order because it is going to be created the butterfly is outlined by the destruction of the number. If it goes time-domain (TD), 1st it's created multiplication and later the total. If it goes frequency-domain (FD), 1st it's created the total so it's created the multiplication. The existent multiplication within the butterfly demands a particular attention, because, if or not it's not enforced expeditiously, it'll degrade the acting of FFT plenty. Basically, there are 2 strategies to try and do the multiplication: to store in a table the trigonometric function values and cos or to form calculations in situ through CORDIC.

#### 4.5Cyclic prefix

The output of the IFFT block [10] is used to make cyclic prefix data. Due to this reason we must have to store the IFFT data at the output RAM (in *Figure 3*). It is necessary that the entire memory has a double size of the cyclic prefix to operate simultaneous read-write mode.

Uses of guard image throughout the guard amount specifically if guard image is chosen to be a prefix extension to every block can cut back quality at

receiver as this convert the linear convolution of the signal and channel to a circular convolution and thereby inflicting the FFT of the circular convolved signal and channel to easily be the merchandise of their individual FFT's. The relative length of the cyclic prefix depends on the quantitative relation of the channel delay unfold to the OFDM image period the explanations to use a cyclic prefix for the guard interval area unit to maintain the receiver carrier synchronization and elimination of silent amount of guard bands. Additionally the circular convolution will be applied between the OFDM signal and also the channel response to model the gear.

## 5.Results

In this section hardware implementation results are discussed

### 5.1FPGA implementation

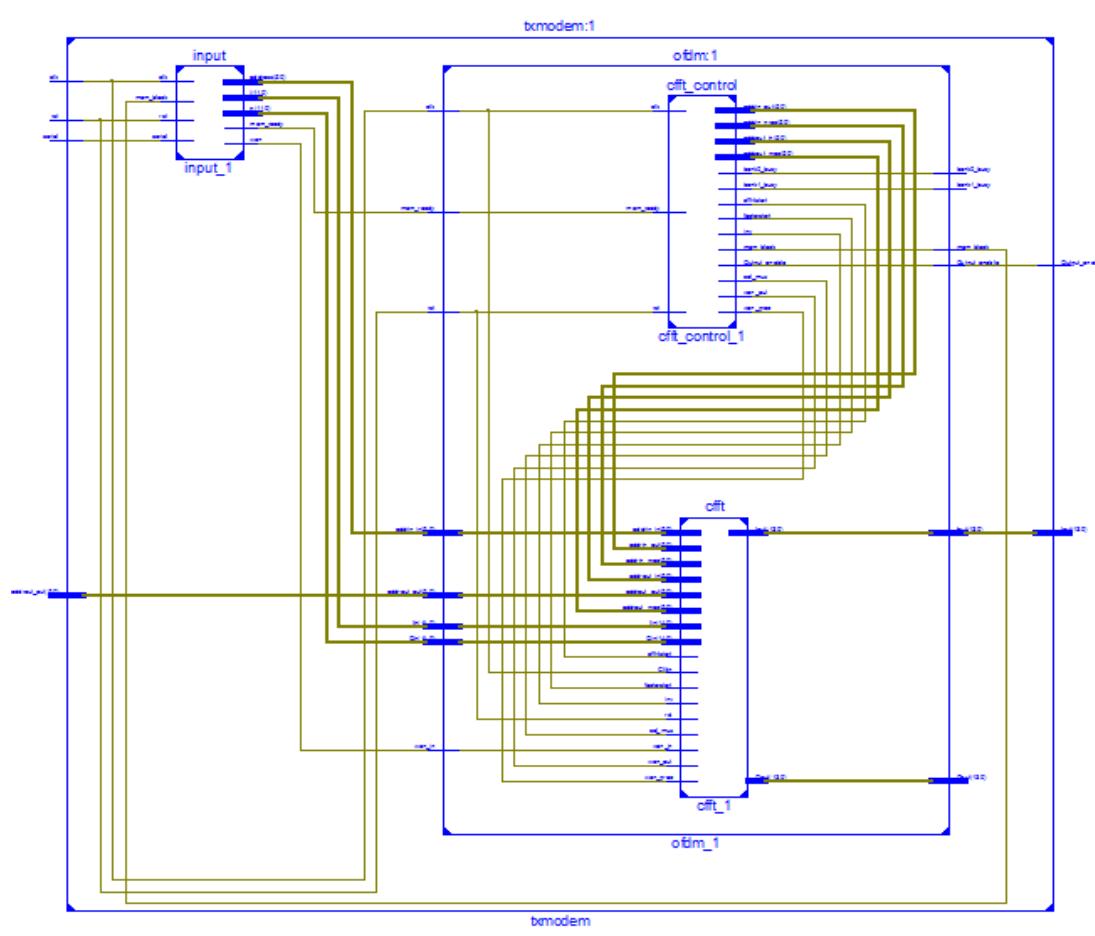
The proposed OFDM architecture is implemented on Spartan-3 FPGA using Xilinx 14.5 tools. The synthesized schematic is given in *Figure 8* which indicates the top view connections and the technology synthesised schematic which indicates the mapping of specific library function is shown in *Figure 9*.

But in FPGA any logic is implemented by mapping those logics into look-up-tables (LUTs) [12]. The technology schematic will give the LUT level block diagram of the proposed architecture.

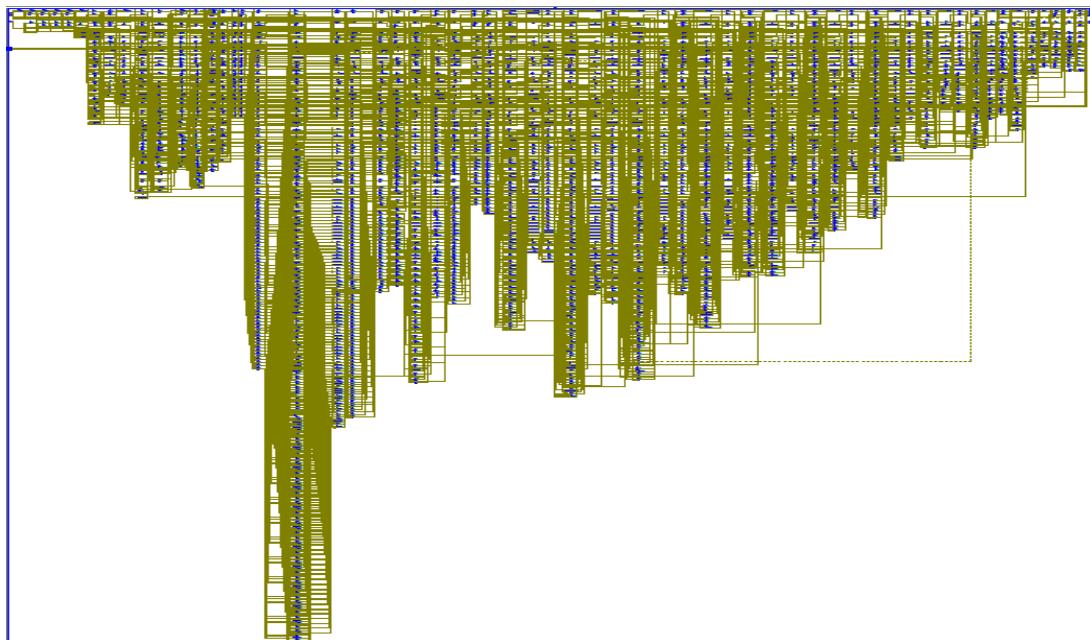
The resource utilization of the proposed architecture is given in *Table 1*. The proposed architecture is implemented on Xilinx Spartan-3 FPGA board. The architecture requires 845 slice flip-flops, 994 LUTs and 5 BRAMs. The architecture can operate on maximum 134.54 MHz clock frequency and the minimum frames durations 192 clocks/frame.

**Table 1** Hardware utilization of the proposed OFDM transmitter

Parameters	Values
Board	Spartan-3 (XC3S1000-4FG320)
Slice Flip-flop	845
4 Input LUTs	994
BRAMS	5
Maximum Frequencies (MHz)	134.54
Minimum Period (ns)	7.431
Minimum Frame Durations (clocks/frame)	192



**Figure 8** Synthesized diagram for proposed OFDM transmitter



**Figure 9** Synthesized technology diagram for proposed OFDM transmitter

### 5.2 Data transmission rates

The proposed OFDM transmitter is designed using 31 channels, each of which is modulated by 4-QAM through IFFT of 64-points. As a result, 192 clock cycles are needed by the transmitter, since the total architecture is implemented in a pipelined fashion. Therefore 192 clocks/frame is the minimum duration of each frame of the proposed design.

However, this is a minimum theoretical estimation of channel rates. The actual rates must be greater than this rate. To calculate the rate first we have to divide the theoretical clock/frame with the number of channels which will give 6.1935 channels/frame. In real implementation this value is approximated to 7 channel/frames, which will give the actual duration 217 clocks/frame. Now if we consider ‘f’ is the operating frequency of the FPGA which is given to the design therefore the duration of each frame will

be  $217/f$ . Since in the proposed architecture, it is implemented by 4-QAM which has 2 bits/channel and 31 channels/frame which resulting 62 bits/frames. This will give the transmission rates as  $\{62/(217f)\}$  bits/second.

### 6. Discussion

In this section we discuss the hardware utilizations of some existing technique and compare those with proposed technique to check the performance. For this purpose we consider the existing techniques presented by Kumar et al. [13] and Julius and Dinh [14]. In both the cases the proposed architecture uses less hardware than existing (*Table 2*). This is mainly due to the optimization of each block at the architecture level and uses of basic logic elements to build the architecture.

**Table 2** Hardware comparison of the proposed OFDM with existing OFDM

Parameters	Kumar et al. [13]	Julius and Dinh [14]	Proposed
Board	Virtex-4	Virtex-4	Spartan-3
Slices	1428	3466	552
Flip-flops	1149	4702	845
4-Input LUTs	2259	4844	994
BRAMs	NA	9	5
DSP48As	NA	16	0
MULT18x18	8	NA	0

NA: Not Available

### 7. Conclusion and future work

In this paper, an efficient FPGA implementation of OFDM transmitter is proposed. The architecture divides any input signal into 31 subcarriers using 64 point modified CORDIC based IFFT. The encoder is the critical part of the system which not only encodes the data, but also control the working of the total block. This architecture is implemented on Spartan-3 FPGA board and the comparison result shows that the proposed architecture is better than existing in terms of hardware utilization. This is mainly due to the simplified version of the logic and the FSM implementation of routing controller which resulted in compact architecture.

In this implementation we have used normal error control coding. For future implementation, trellis-coded modulation (TCM) and Viterbi decoder can be used to replace the normal error control coding architecture for better transmission accuracy. Then different kinds of multicarrier system can be implemented to overcome ISI and inter-channel interference (ICI). It decreases the channel capacity. The effect of ICI is greater than ISI. To overcome

this problem, different kinds of multicarrier systems can be used in future.

### Acknowledgment

None.

### Conflicts of interest

The authors have no conflicts of interest to declare.

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