A Single Stage Low Gain Pseudo Differential Class-AB telescopic Cascoded Op-amp for Pipelined ADC

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Abstract

In this paper, a low gain pseudo differential class-AB telescopic op-amp for pipelined ADC is presented. By applying split capacitor CDS technique in a pipelined ADC, finite op-amp gain errors of low gain op-amps are eliminated. This significantly reduces the power consumption of the pipelined ADC. A pseudo differential class AB opamp is chosen as the suitable op-amp topology because of its high power efficiency and large signal swing compared to other topologies. Additional class AB capacitors used further enhances the DC gain and bandwidth of the amplifier.

Keywords

pseudo differential, class AB, split capacitor CDS, pipelined analog to digital converter, telescopic

1. Introduction

A conventional pipelined ADC requires high gain opamps for accurate signal processing. This makes it unsuitable for low power applications. The split capacitor CDS technique is used in pipelined ADC [2] to avoid using of high gain amplifiers by correcting finite op-amp gain error in low gain opamps.

Operational amplifier is the heart of any analog circuit. Speed, gain, power amongst other performance parameters presents contradictory choices for op-amp architectures. Telescopic cascoded op-amp has better bandwidth and lower power consumption than other op-amp topologies. Applying pseudo differential-class-AB approach to a telescopic-cascode op-amp enhances the effective values of the slew rate and thereby reduces the power consumption. The class-AB capacitors used in the op-amp enhance the dc gain and bandwidth of the amplifier

In this paper section II describes the op-amp architecture. Section III gives the simulation results.

Finally, Section IV gives summary based on the simulation results.

2. Op-amp structure

Efficient class AB architecture for single stage operational amplifiers is presented in this paper. Applying the pseudo differential class AB approach to op-amp enhances the effective values of slew rate and transconductance.

Figure 1 shows the architecture of pseudo differential class AB telescopic op-amp. The structure employs a switched capacitor level shifter to provide a signal-dependent current in the current source of the common-source amplifier [3].



Fig.1: Pseudo differential class-AB telescopic cascoded op-amp

The transconductance of the single stage op-amp is proportional to $C_L/T_{SETTILING}$, where C_L is the output loading and $T_{SETTILING}$ is the settling time. The equivalent transconductance Gm of the amplifier is given by

Gm = gmN + gmP(C1+C2) / (CP + C1 + C2) (1) The equivalent transconductance is proportional to the ratio of the parasitic capacitor of PMOS *Cp* and the class-AB capacitor (*C*1 + *C*2).

The structure will improve the equivalent value of the stage transconductance leading to more gain and bandwidth for the op-amp. This is an important advantage of this structure. The main drawback of the International Journal of Advanced Computer Research (ISSN (print): 2249-7277 ISSN (online): 2277-7970) Volume-2 Number-4 Issue-6 December-2012

structure presented here is the comparatively large capacitor utilized for level shifting.

3. Design procedure

For a supply voltage of 1.8V an initial power budget of 1mW was allotted, which gives total biasing current of 0.5 mA. This is the total current from rail to rail which should be divided into two branches. Then 0.25mA was distributed between two branches of the telescopic op-amp. Generally, the overdrive of PMOS should be higher than NMOS as mobility of PMOS is approx. 2.5 times less than NMOS. We decided to start with Vod of PMOS as 270 mV and Vod of NMOS as 180 mV after a careful analysis.

Initial W/L values (in um) can be chosen by using the current expression in saturation region operation. We assumed $\mu_n \ ^*C_{ox} = 150 \ uA/V2$ and $\mu_p \ ^*C_{ox} = 60 \ uA/V2$ for first iteration. The saturation region current expression helps us in calculating the aspect ratios (W/L) of transistors as the current through them is known and overdrive voltage is assigned.

$$I_{\rm D} = \frac{\mu n C \text{ ox}}{2} \left(\frac{W}{L}\right) [Vgs - Vt]^2$$
⁽²⁾

Here I_D is the biasing current, µn and C_{ox} are process parameters, W/L is aspect ratio of a transistor, Vgs is gate-source voltage and V_T is threshold voltage of device. The circuits were simulated in a 0.18um CMOS technology with Cadence. The op-amps were designed with load capacitances 8pF for a 2MHz input signal. The body terminal of all NMOS and PMOS transistors were connected to the VSS and VDD, respectively.

4. Simulation results

Transient analysis of the Op-amp:

The pseudo differential class-AB telescopic op-amp was designed and simulated using CADENCE virtuoso 180nm technology. The schematic for the pseudo differential telescopic op-amp is shown in figure 2.



Fig. 2: Schematic for pseudodifferential class-AB telescopic cascoded op-amp

A 2Mhz input of 1.6 volts peak to peak is given to the op-amp and the transient response was plotted using cadence virtuoso. Figure 3 gives the transient waveform of the pseudodifferential class-AB telescopic cascaded op-amp.

AC analysis of the Op-amp:

AC analysis of the op-amp is done with a 2 Mhz input of 1.6 volts peak to peak and AC response was plotted. Figure 4 shows the AC response of the pseudo differential class- AB telescopic op-amp. From the figure 4, it is observed that a dc gain of 29.19 dB is obtained. A phase margin of 180° is obtained for pseudo differential class- AB telescopic op-amp op-amp as shown in the figure. The maximum slew rate that can be obtained by the op- $2\pi V peak f_{max}$ which is amp is given by 2*3.14*1.6*2M, that is 22.6 v/ μ s. The slew rate of the pseudodifferential telescopic cascaded op-amp is given by Itail/CL where Itail is the tail current and CL is the load capacitance. The slew rate obtained is 15.790 v/µs.

with minor modification.



Fig. 3: Transient response of pseudodifferential class-AB telescopic cascoded op-amp.



Fig .4 : AC response of pseudodifferential class-AB telescopic cascoded op-amp.

Table 1 shows the performance summary of pseudo differential class- AB tlescopic op-amp op-amp.

Input Range	1 .6Vpp Differential
Power Supply	1.8v
Technology	180 nm Technology
DC gain	29.16 Db
Phase	180^{0}
Power Consumption	0.2mW

Table.1: Performance summary of the op-amp

5. Conclusion

A power-efficient class-AB pseudo differential telescopic cascoded op-amp has been developed to reduce the power consumption of the pipelined ADC using split capacitor CDS technique and op-amp sharing technique. The split capacitor CDS technique

corrects the op-amp gain error allowing usage of low gain op-amps. class-AB pseudo differential telescopic cascoded op-amp has been chosen because of its high power efficiency and large signal swing. The class-AB capacitors have also been employed to enhance the bandwidth and dc gain of this op-amp

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References

- K. Gulati and H.-S. Lee, "A High-Swing CMOS Telescopic Operational Amplifier," in *IEEE Journal of Solid-State Circuits*, Vol. 33, No. 12, pg. 2010, December 1998.
- [2] Jin-Fu Lin, Soon-Jyh Chang, Chun-Cheng Liu, Chih-Hao Huang, "A 10-bit 60-MS/s Low-Power Pipelined ADC With Split-Capacitor CDS Technique", in IEEE transactions on circuits and systems—ii: express briefs, vol. 57, no. 3, march 2010.
- [3] Taherzadeh-Sani, M, Lotfi, R., Shoaei, O, "A pseudo-class-AB telescopic-cascode operational amplifier", in IEEE transactions on circuits and systems-Vol 1, pg. 737-40, May 2004.
- [4] S. Mehrmanesh, H. A. Aslanzadeh, M. B. Vahidfar, and M. Atarodi, "A 1.5 V high-speed class AB operational amplifier for highresolution high-speed pipelined AD converters," in Proc. 2003 IEEE Int. Symp. Circuits System, May 2003, Vol. 1, pp. 273-276.
- [5] J. Ramirez-Angulo, R. G. Carvajal, A. Torralba, and C. Nieva, "A new class *AB* differential input stage for implementation of low-voltage high slew-rate opamps and linear transconductors," in *Proc. 2001 IEEE Int. Symp. Circuirs Systems*, May 2001, Vol. 1, pp.671-674
- [6] R. Lotfi and O. Shoaei, "A low-voltage lowpower fast-settling operational amplifier for use in high-speed high-resolution pipelined A/D converters," *IEEE Intl. Symp. Circuits & Systems, ISCAS 2002*, vol.II, pp. 416-419, 2002.
- [7] J. N. Babanezad, "A low-output-impedance fully differential op amp with large output swing and continuous-time common-mode feedback," *IEEE J. Solid-State Circuits*, vol. 26, pp. 1825–1833, Dec. 1991.
- [8] K. Bult and G. J. G. M. Geelen, "A fast-settling CMOS op amp for SC circuits with 90-dB DC gain," *IEEE J. Solid-State Circuits*, vol. 25, pp.1379–1384, 1990

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